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Enabling the Electronics Revolution

High Speed Cable Solutions for Data Center Application

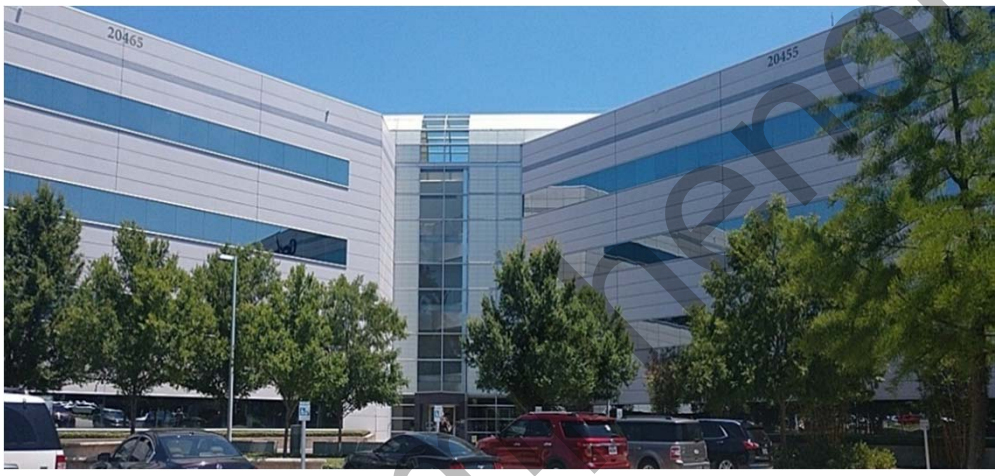
Amphenol Interconnect and Sensor System(AISS)

Amphenol AssembleTech(AST)

August 26, 2021

Amphenol AssembleTech (AST)
Xiamen, China / Houston, USA/Ho Chi Minh, Vietnam

AST Xiamen, China



AST Houston, USA

AST Ho Chi Minh, Vietnam

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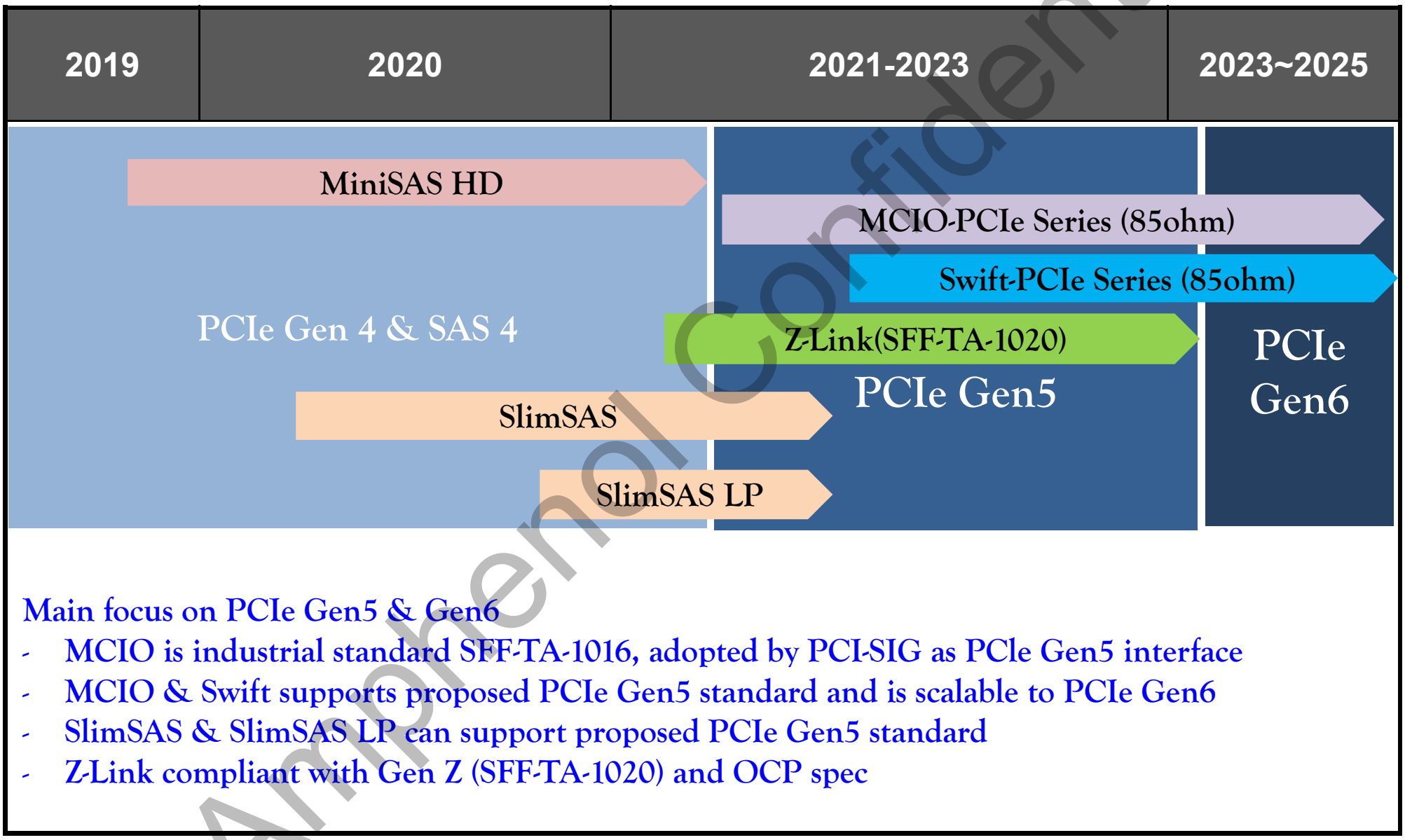
Product Roadmap for PCIe



Main focus on PCIe Gen5 & Gen6

- MCIO is industrial standard SFF-TA-1016, adopted by PCI-SIG as PCIe Gen5 interface
- MCIO & Swift supports proposed PCIe Gen5 standard and is scalable to PCIe Gen6
- SlimSAS & SlimSAS LP can support proposed PCIe Gen5 standard
- Z-Link compliant with Gen Z (SFF-TA-1020) and OCP spec

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Product Roadmap for Data Rates

PCIe Gen4 16G
- SlimSAS
- SlimSAS LP
- OCuLink

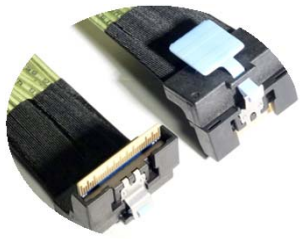
SAS 4.0 24G
- SlimSAS
- SlimSAS LP
- OCuLink

OpenCAPI 25G
- SlimSAS
- SlimSAS LP

PCIe Gen5 32G
- MCIO
- Swift
- SlimSAS LP
- SlimSAS
- Z-Link(Gen-Z)

PCIe Gen6 64G
- Swift
- Swift DE
- MCIO
- Lightyear

PAM4 56-112G
- MCIO
- Swift
- Flash
- Z-Link(Gen-Z)
- Lightyear

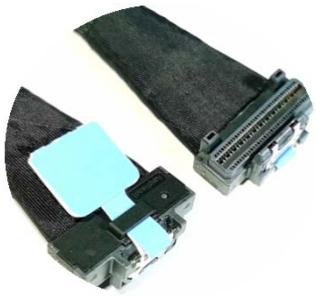


SlimSAS

SlimSAS LP

Z-Link

MCIO



Swift

Flash

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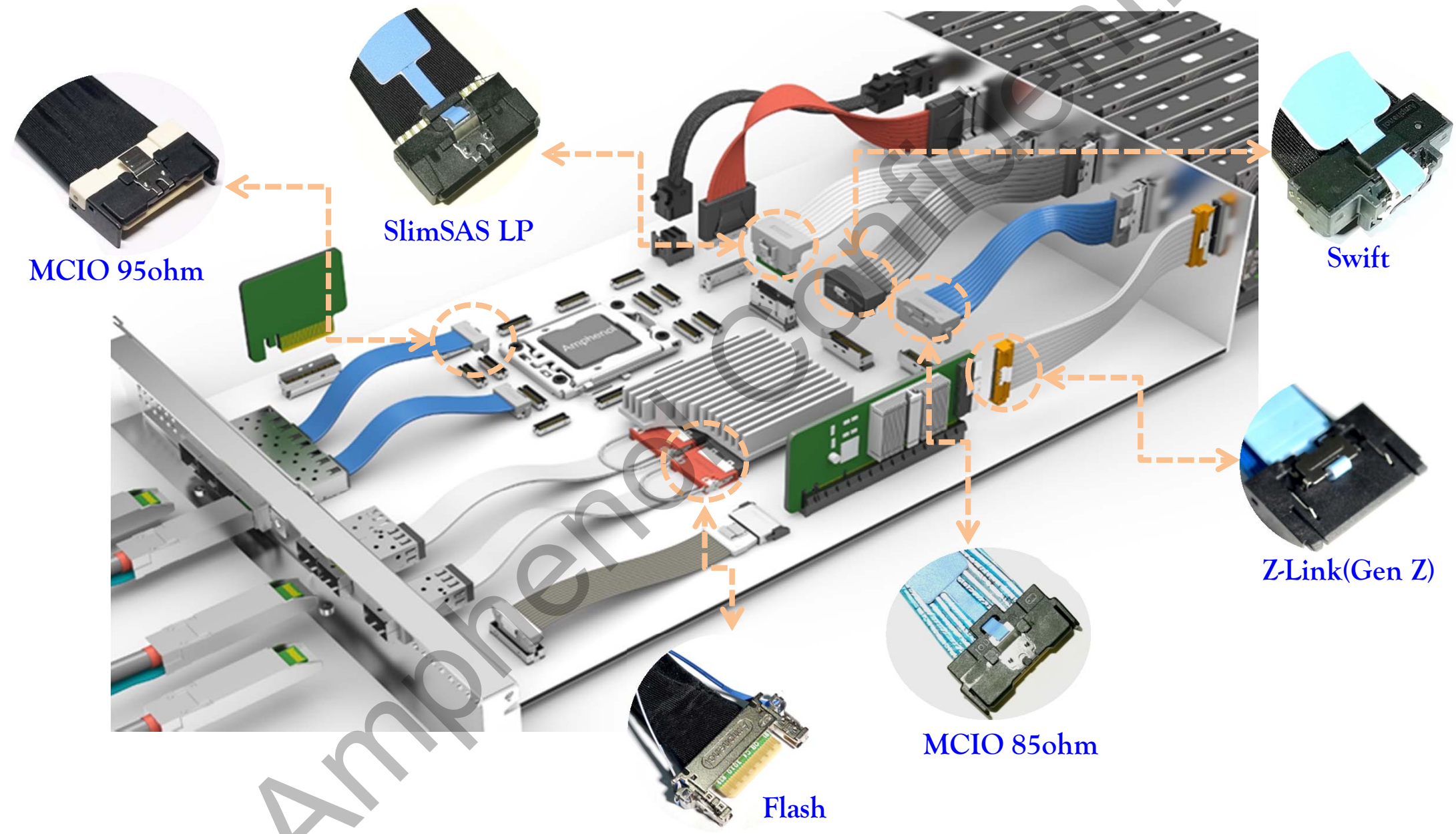
Product Application

Chip to Backplane & to IO



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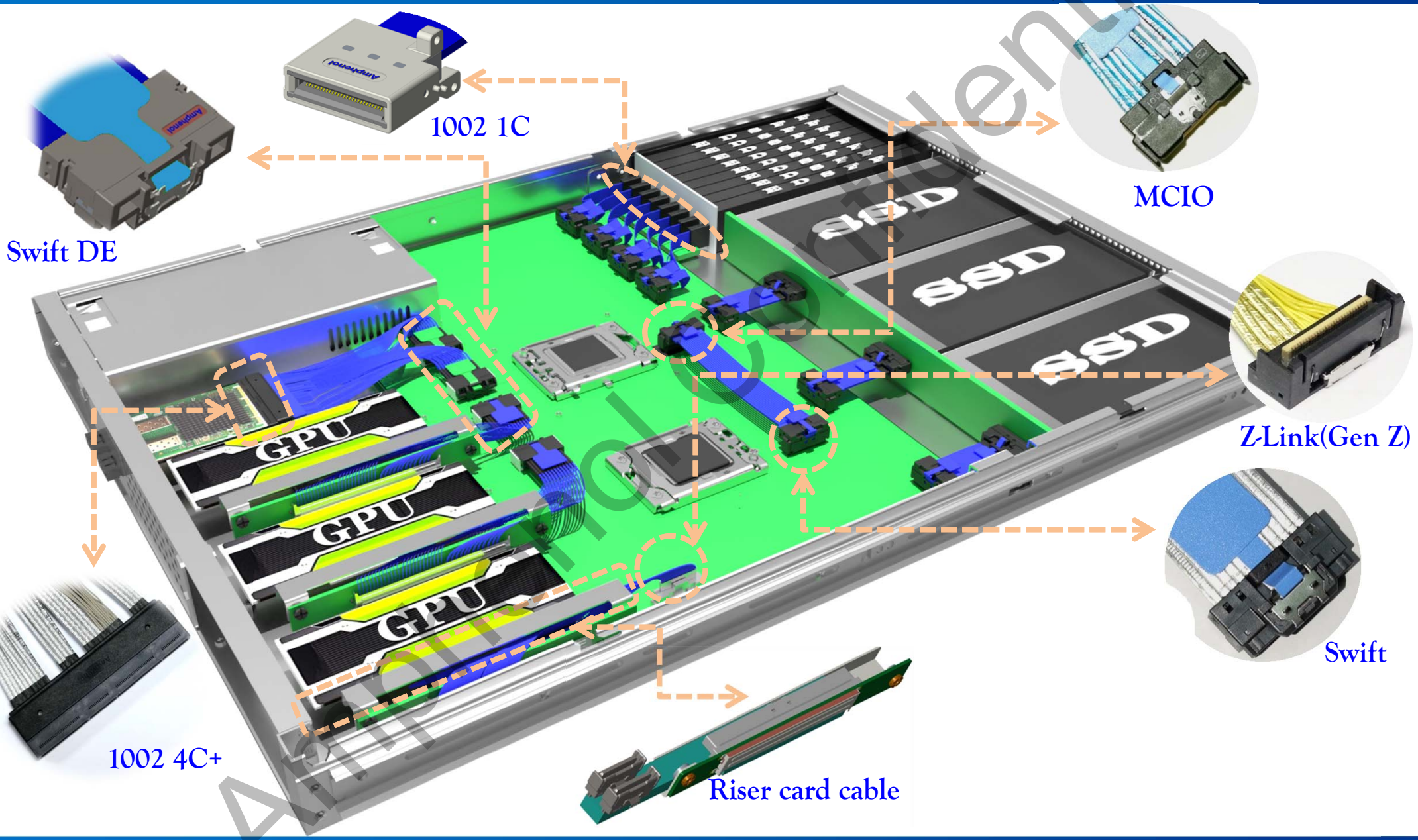
Product Application

Chip to riser card & to chip & to EDSFF and OCP NIC3.0



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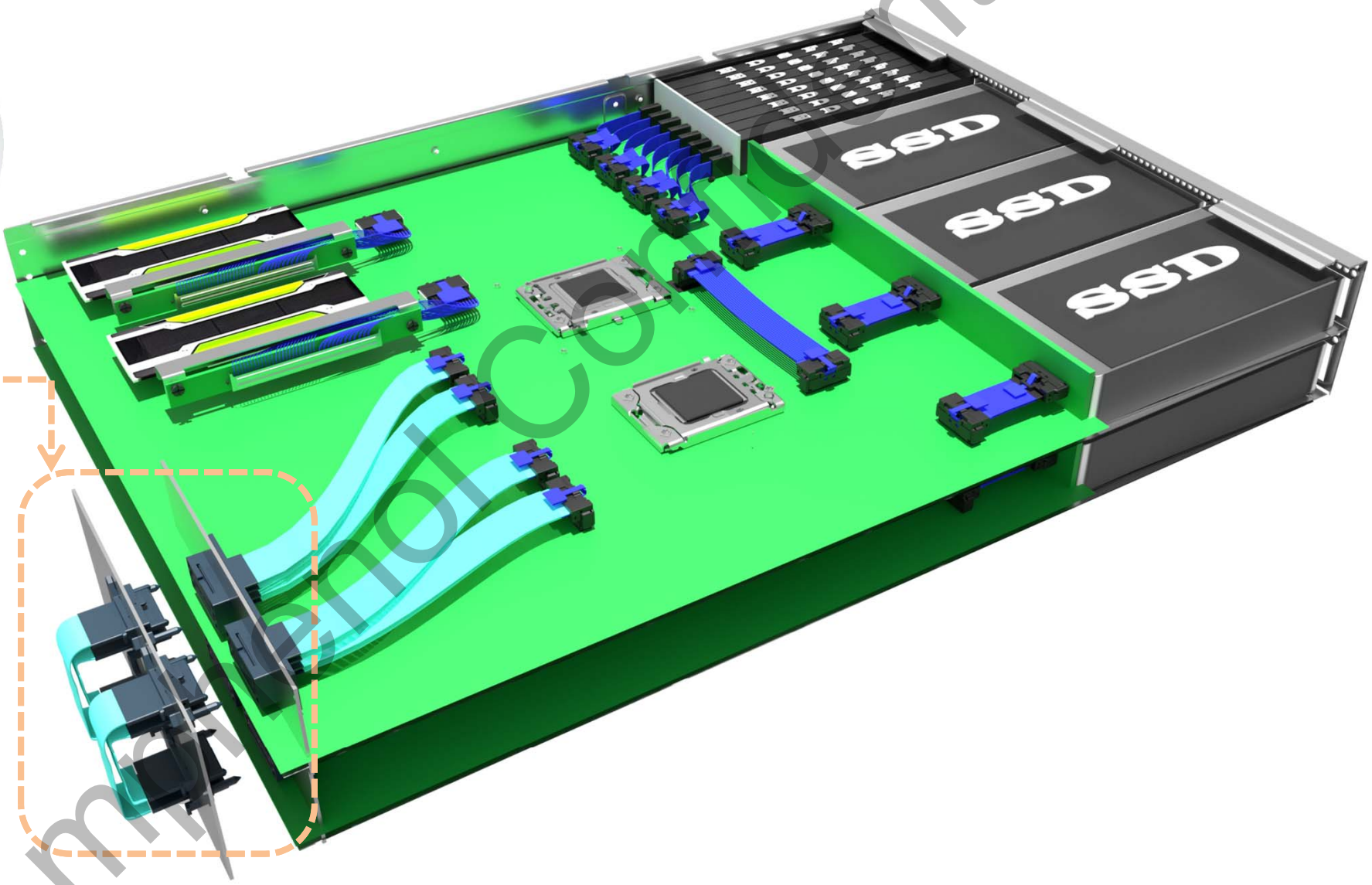
Product Application

High speed connection between multiple mother boards

Blind Mate



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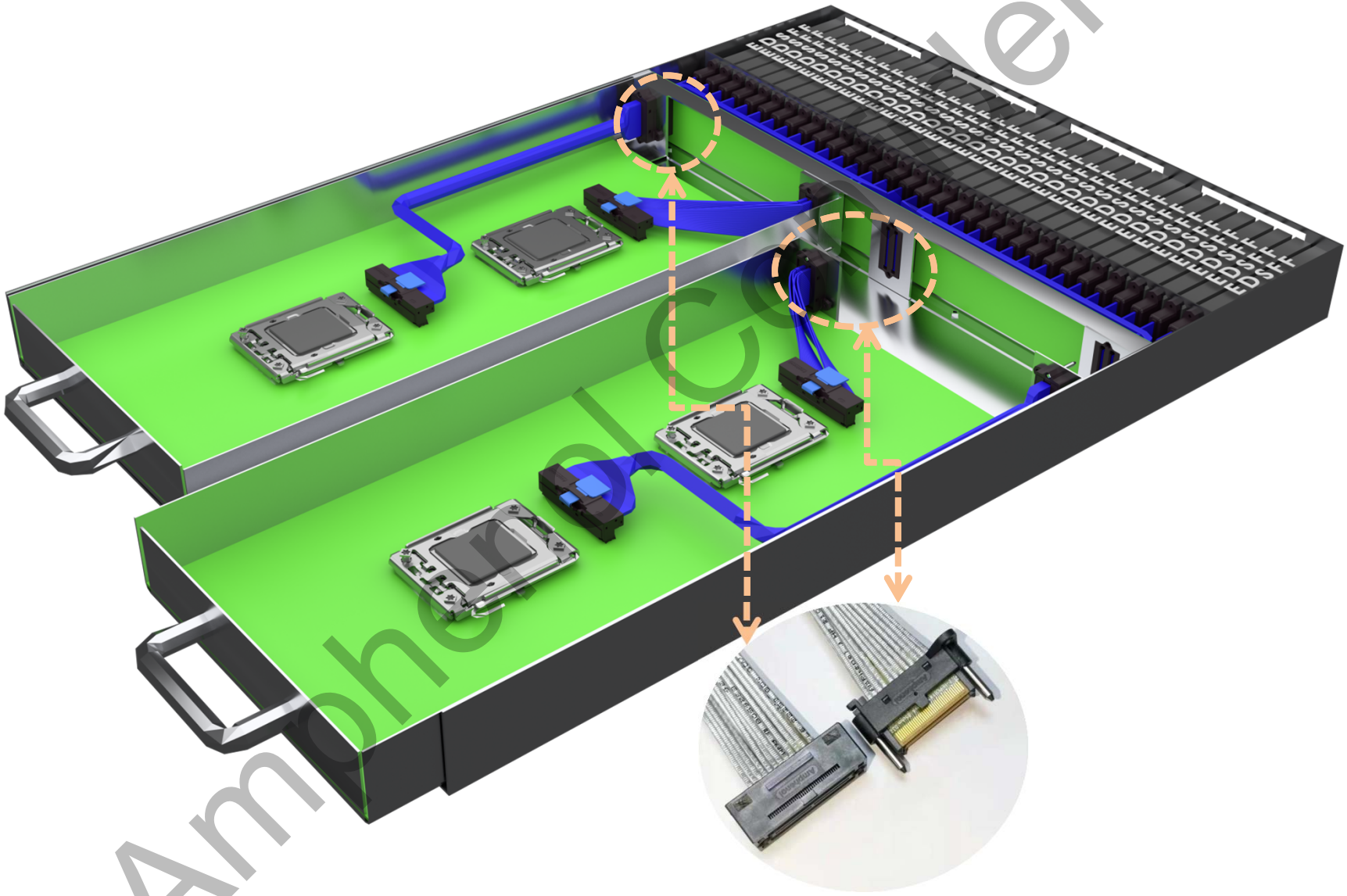
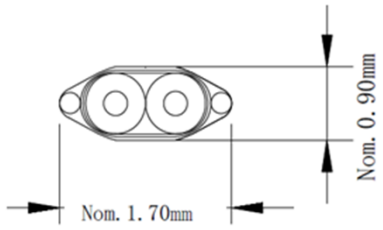
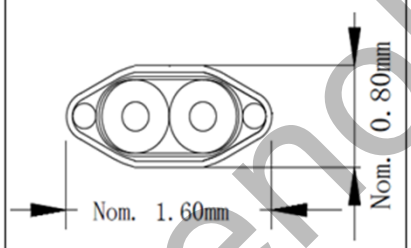
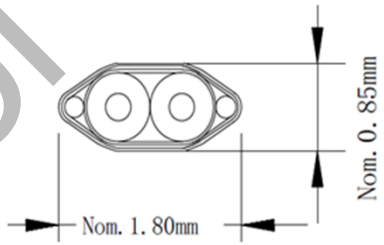
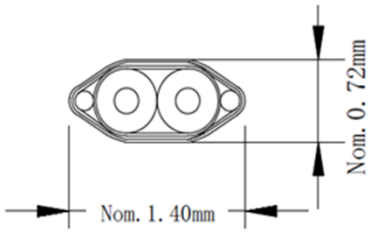
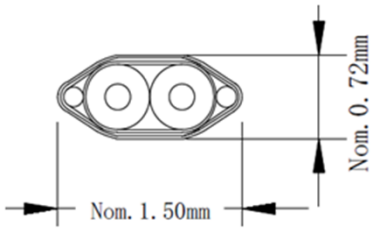
Application: Chip to backplane



Raw Cable Options for PCIe Gen5&Gen6

Class	Premium-1	Premium-2	Premium-3	Premium-4	Premium-5
			Nominal Loss / meter		
4GHz	-2.60	-3.00	-2.70	-3.70	-3.80
8GHz	-3.80	-4.50	-3.90	-5.50	-5.60
16GHz	-5.30	-6.20	-6.85	-7.80	-9.10
Drain Type	Dual-Drain	Dual-Drain	Dual-Drain	Dual-Drain	Dual-Drain
Wire Gauge	30AWG	30AWG	30AWG	32AWG	32AWG
Cross Section Dimension					

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Extremeport-Swift

Swift

Swift mating height is less than 9mm and is scalable to reach data rates up to PCIe Gen6. Swift features a mechanically robust lead frame design with two guide PINs and is available in multiple pin configurations to support different applications.

SI

- Supports proposed PCIe Gen5
- Scalable to support PCIe Gen6, SFF-TA-1002 112G PAM4

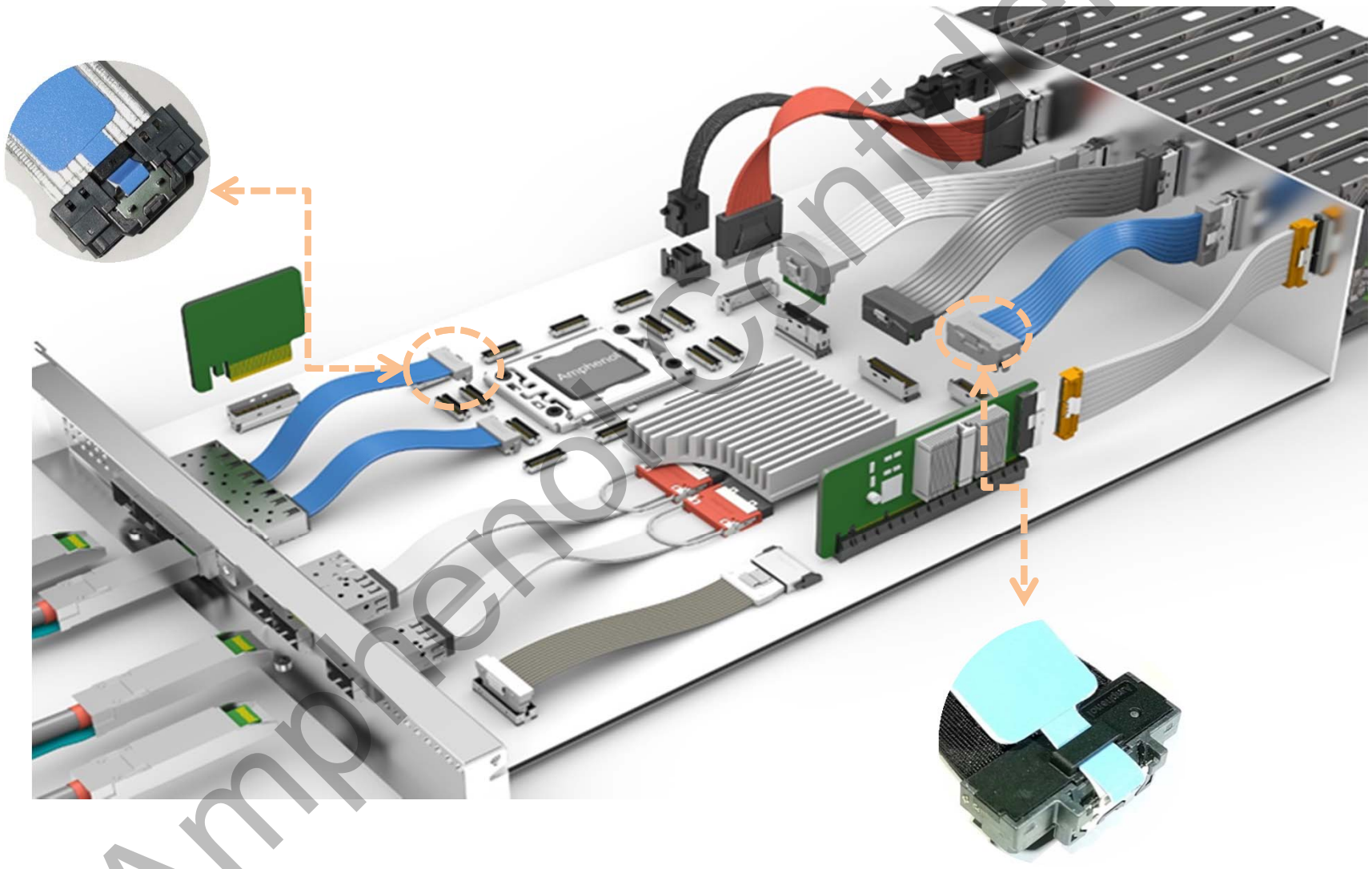
Mechanical

- Mating height less than 9mm
- Mechanically robust with dual guide PIN feature

Application

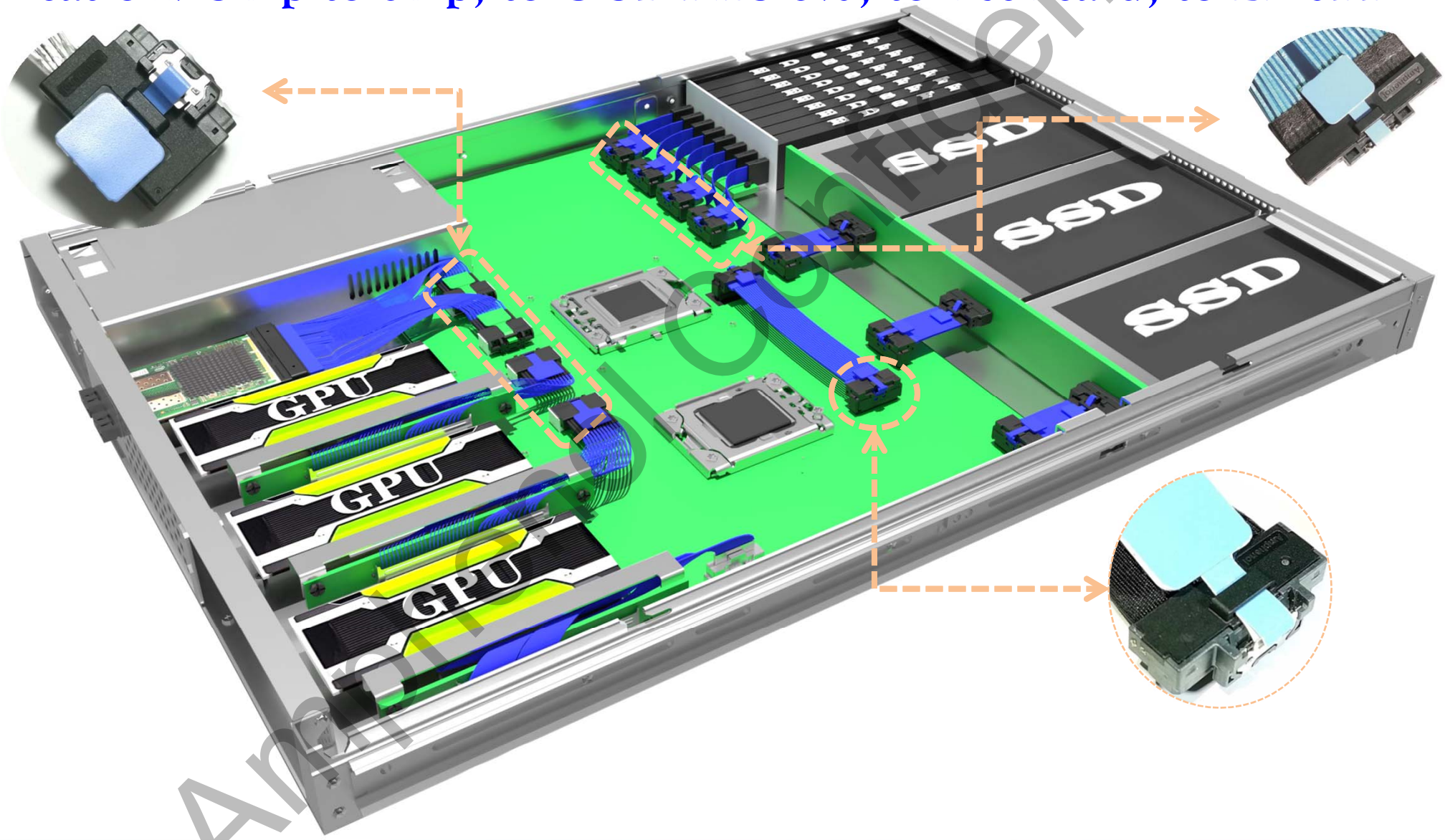
- Supports chip to IO, chip to chip, chip to riser
- Supports chip to OCP NIC3.0, chip to EDSFF

Applications: Chip to IO, chip to backplane



Swift

Application: Chip to chip, to OCP NIC 3.0, to riser card, to EDSFF



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Swift

Benefits of application

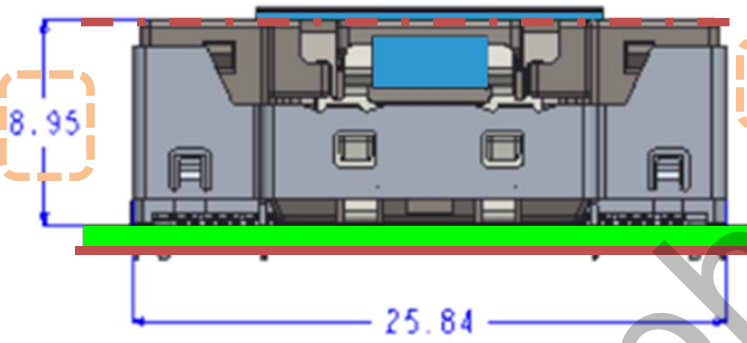
- **Excellent SI**
  - Supports proposed PCIe Gen5
  - Scalable to support PCIe Gen6 and SFF-TA-1002 112G PAM4
- **Connector Type**
  - Supports 38p, 74p, 124p, 148p, and STR, RA, SE
- **Diversified applications**
  - Chip to chip, chip to riser, chip to backplane and chip to IO

Swift

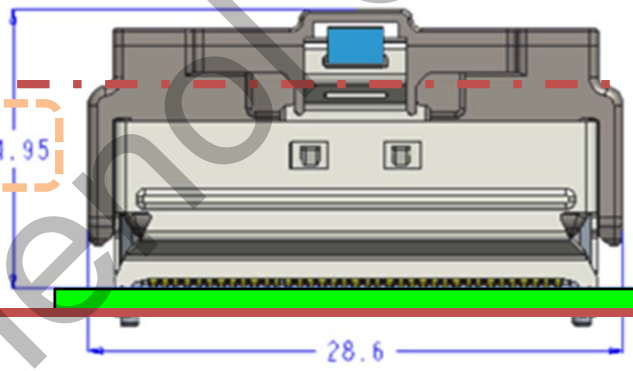
Mechanical: Extreme low mating height

Z-Link is 7.8mm(87%) higher than Swift
MCIO is 6mm(67%) higher than Swift

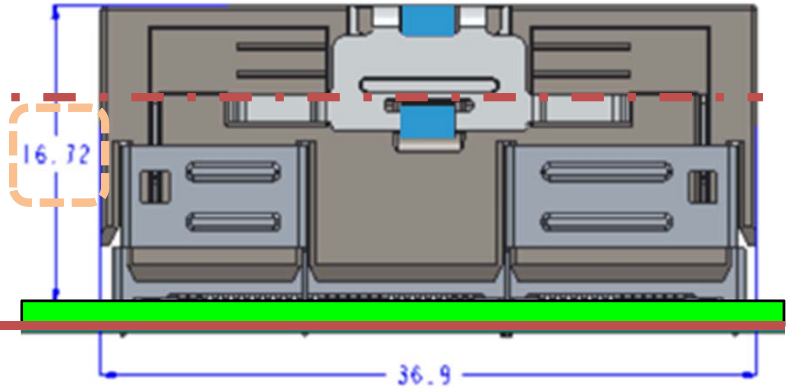
Swift 74pin



MCIO 74pin



Z-Link 84pin



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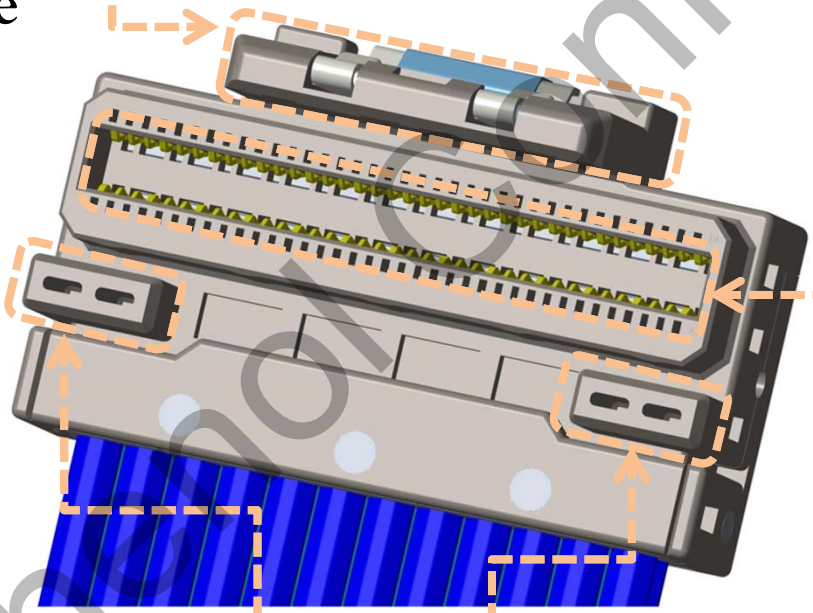
Mechanical: Lead frame, guide PIN, anti-reverse guide feature



Swift

Benefits of mechanical

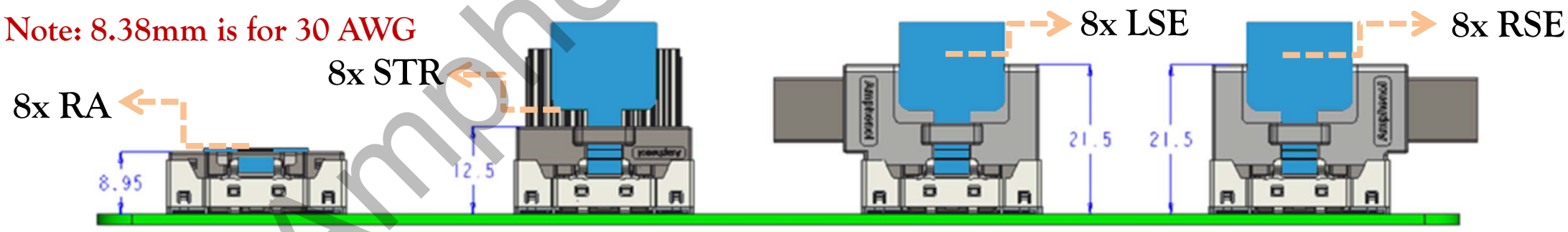
- **Small Size** — Extreme low mating height 8.95mm
- **Robust** — Guide PIN and anti-reverse feature
- **Optimized process** — Lead frame terminal design

Configuration

Swift

Configuration		Plug						Receptacle	
Type	Positions	Impedance	Straight	Right Angle	Right Side Exit	Left Side Exit		Impedance	Vertical
6X	38	85	tool on request					85	tool on request
12X	74		Available						Available
20X	124		In roadmap Q4	Available	tool on request				Available
24X	148		tool on request						tool on request

Note: 8.38mm is for 30 AWG



Swift

Highlight

SI

- Supports proposed PCIe Gen5 standard
- Scalable to support PCIe Gen6 and SFF-TA-1002 112G PAM4

Mechanical

- Robuster, mating height 8.95mm

Application

- Supports multiple connector types to optimize cable routing

Extremeport-Swift DE (Dual Exit)

Swift DE

Swift DE has a mating height of less than 10mm, supports proposed PCIe Gen5 and is scalable to Gen6. The single receptacle design, mates with both RA and reversed RA plug while maintaining the same overall mating height while including an anti-reverse mating feature.

SI

- **Supports proposed PCIe Gen5 standard**
- **Scalable to support PCIe Gen6 and SFF-TA-1002 112G PAM4**

Mechanical

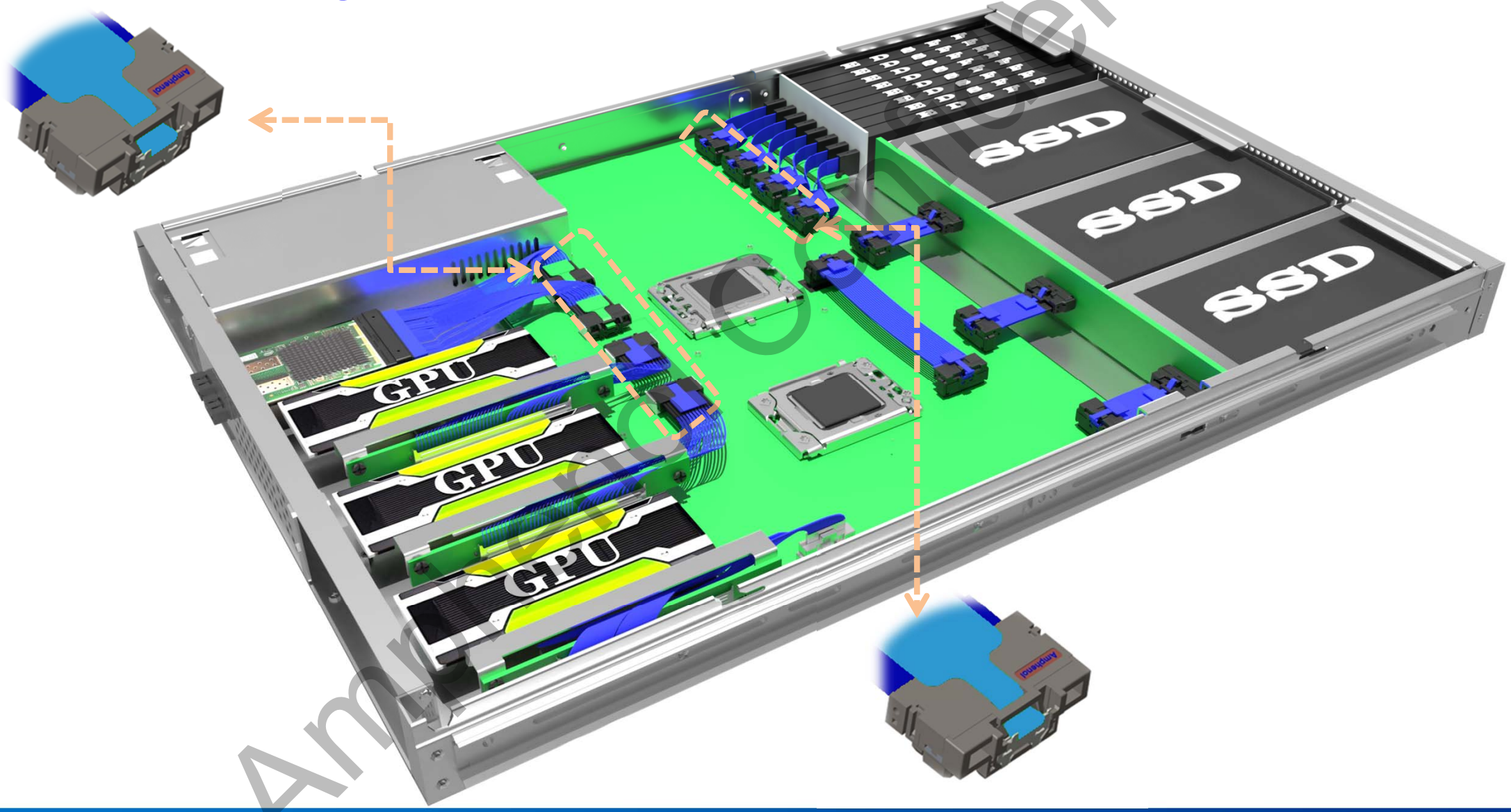
- **RA and reversed RA will keep same mating height 9.6mm**

Application

- **Supports chip to IO, chip to chip, chip to riser card**

Swift DE

Applications: High density layout



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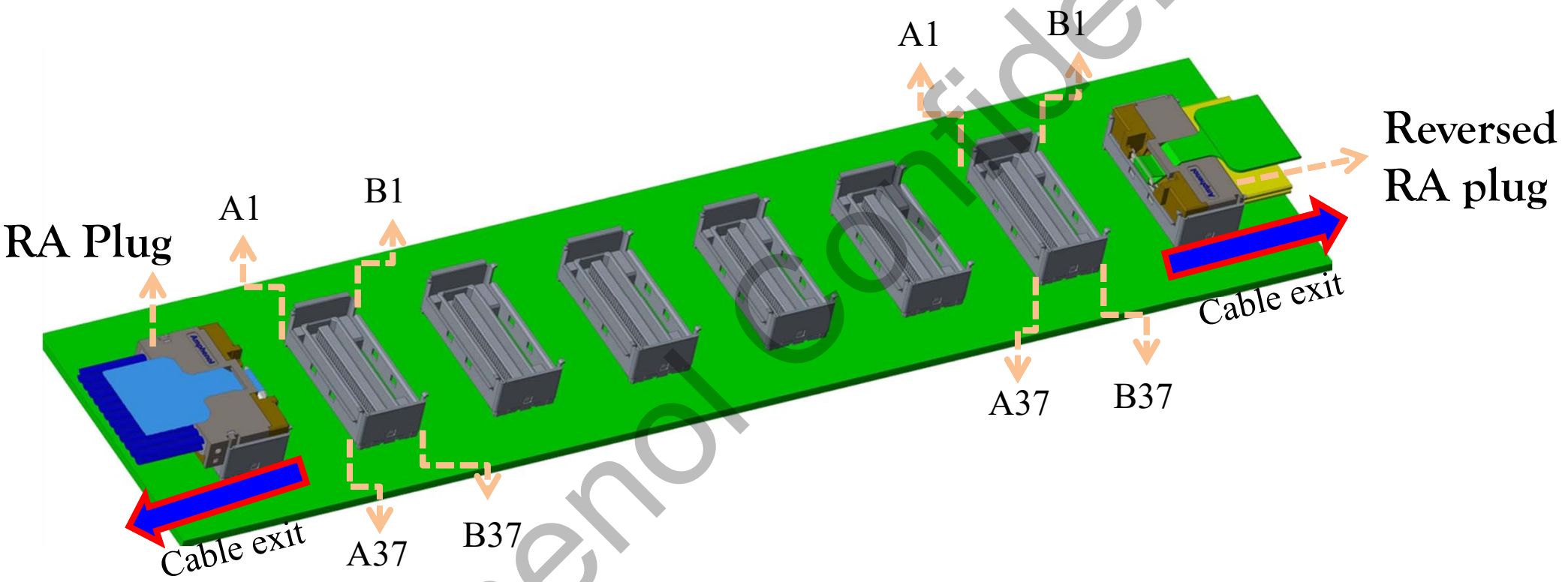
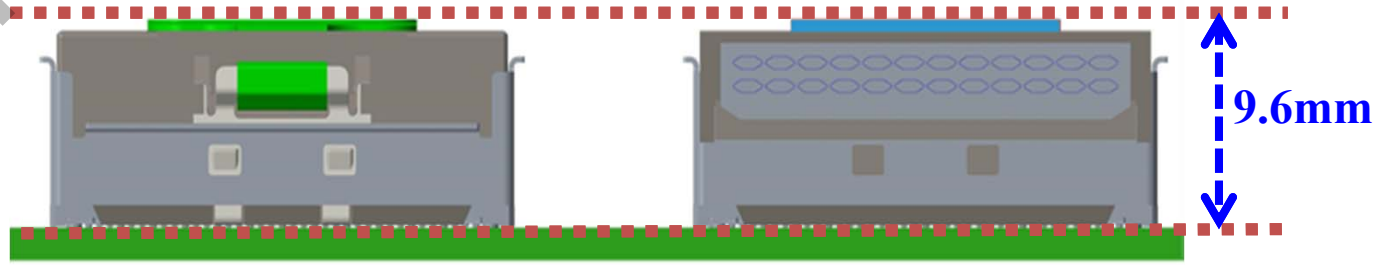
Swift DE

Benefits of application

- **Excellent SI**
  - Supports proposed PCIe Gen5 standard
  - Scalable to support PCIe Gen6 and SFF- TA-1002 112G PAM4
- **Bidirectional exit**
  - RA and reversed RA supports bidirectional cable exit
- **Diversified applications**
  - Chip to IO, chip to riser, chip to backplane, chip to chip

Mechanical: Same receptacle for RA and reversed RA





Swift DE

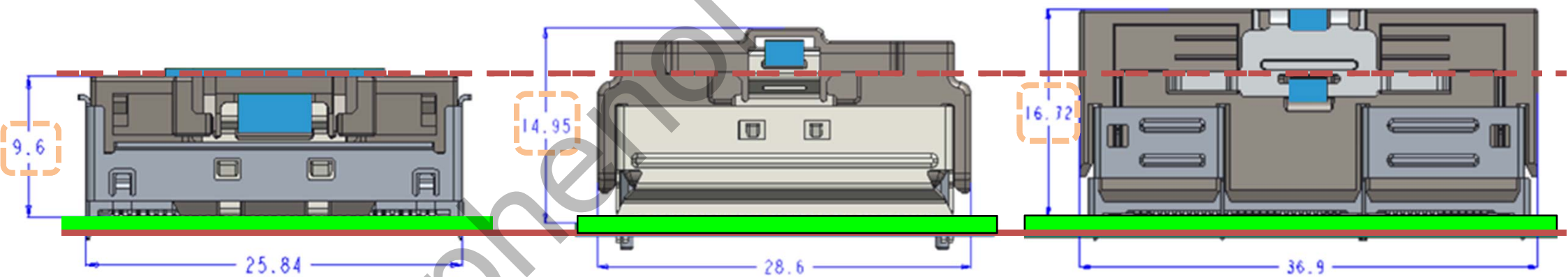
Mechanical: Low mating height

Z-Link is 7.12mm(74%) higher than Swift DE
MCIO is 5.3mm(56%) higher than Swift DE

Swift DE 74pin

MCIO 74pin

Z-Link 84pin



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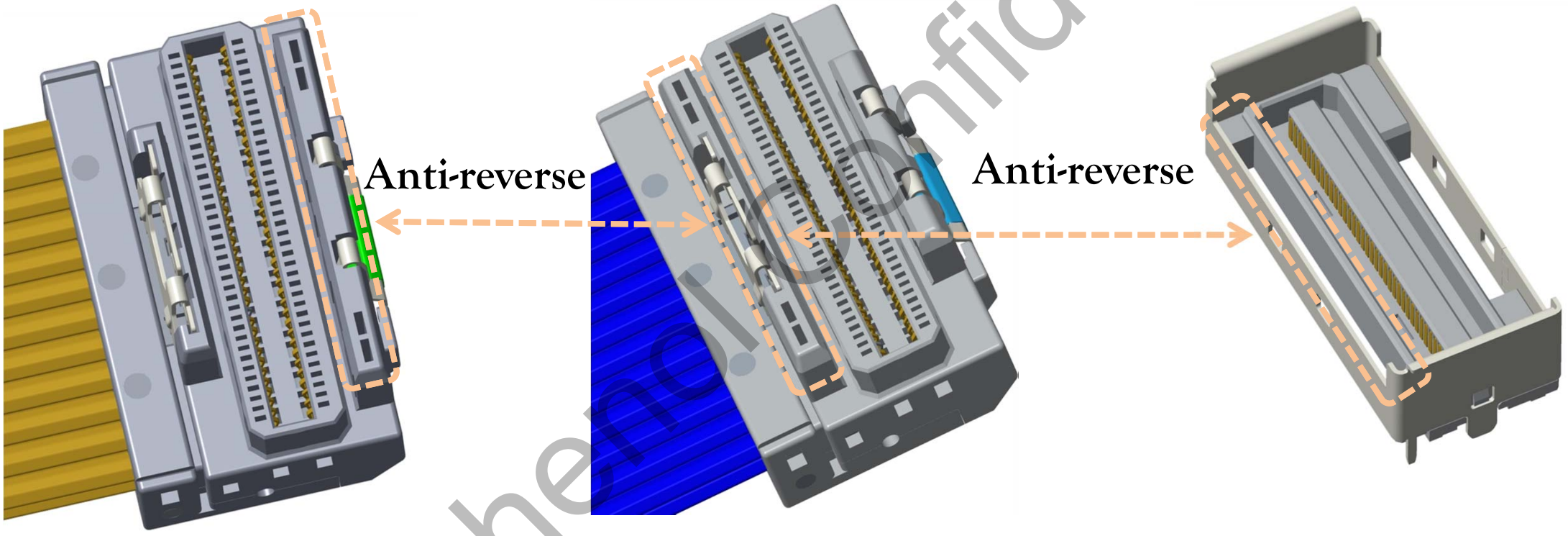
Mechanical: Anti-reverse feature



Reversed RA plug

RA plug

Vertical board connector

Swift DE

Benefits of mechanical

- **Small size** — RA and reversed RA has same mating height(9.6mm)
- **Robust** — Anti-reverse feature prevents pin crash during mating process
- **Double lock** — Supports two passive latches(or 1 active latch+1 passive latch)

Configuration matrix

Swift DE									
Configuration		Plug							Receptacle
Type	Positions	Impedance	RA	Reversed RA	Straight	Right SE	Left SE	Impedance	Vertical
6X	38	85ohm	tool on request					85ohm	tool on request
12X	74		2021,Q4	2021,Q4	tool on request				2021,Q4
20X	124		tool on request						tool on request
24X	148		tool on request						

Swift DE

Highlight

SI

- Supports proposed PCIe Gen5 standard
- Scalable to support PCIe Gen6 and SFF-TA-1002 112G PAM4

Mechanical

- RA and reversed RA with anti-reverse feature, mate with same receptacle and keep same height, double latch mechanism

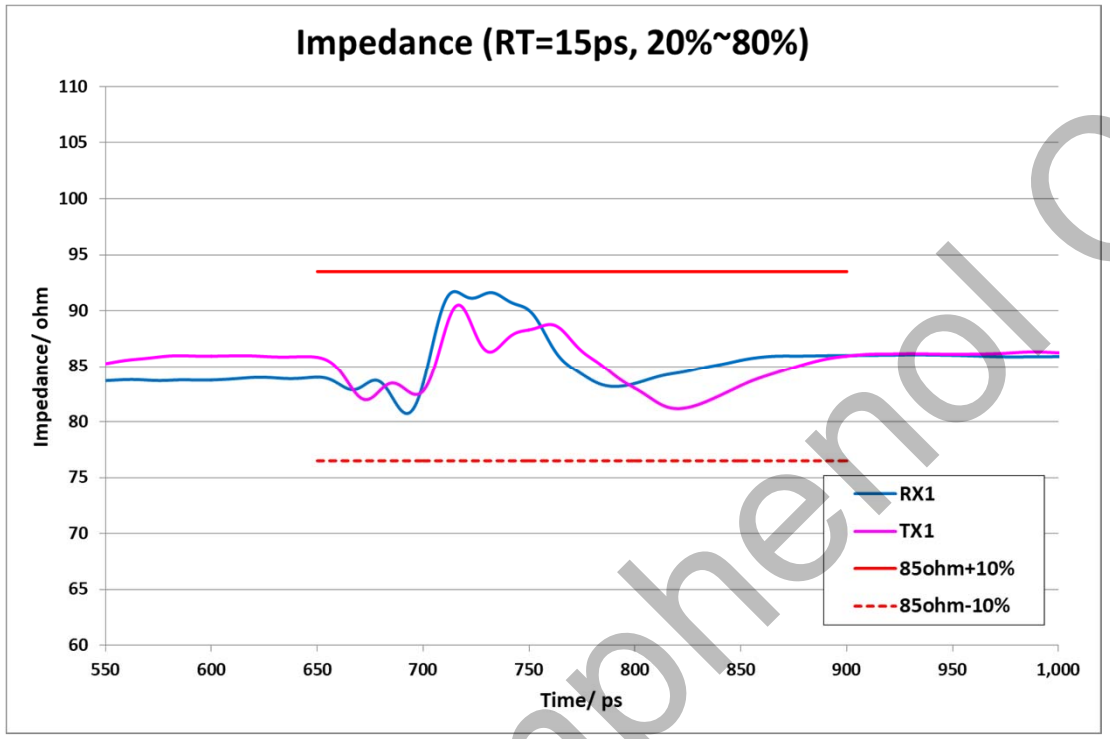
Application

- Supports high density layout with bidirectional cable exit

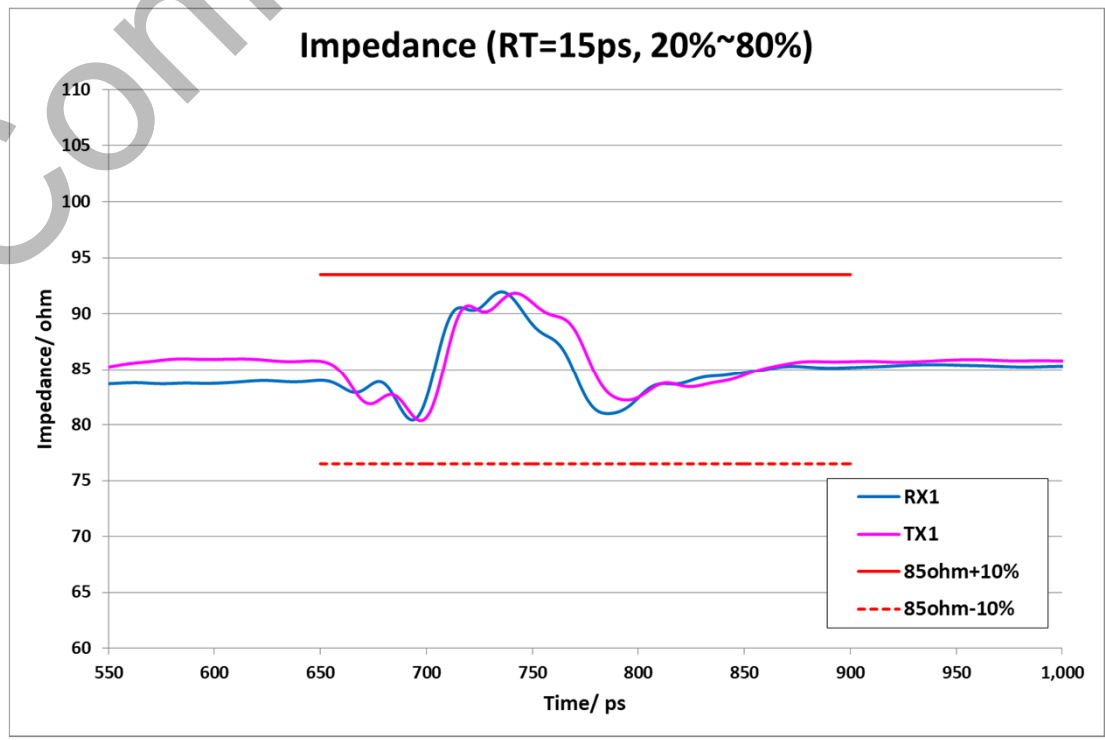
Swift & Swift DE_PCIe Gen5

SI measured data based on proposed PCIe Gen5 standard, 1000mm 29AWG cable, RA-RA vs. STR-STR

RA Plug



STR Plug



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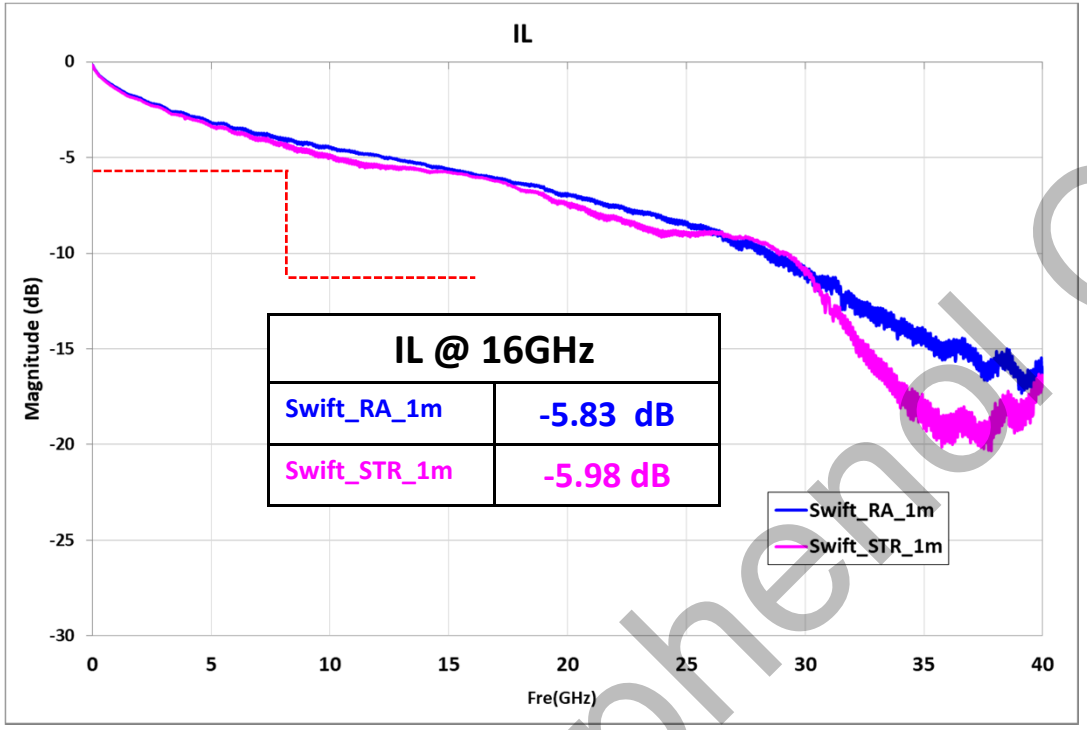
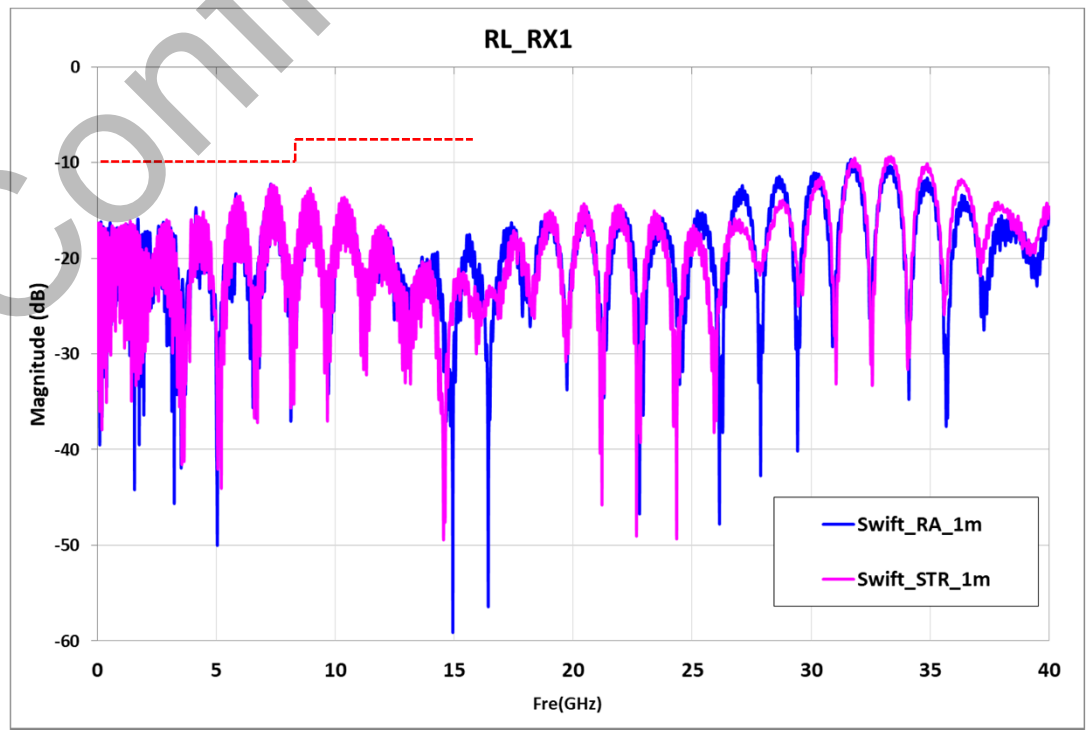
Swift & Swift DE_PCIe Gen5

SI measured data based on proposed PCIe Gen5 standard, 1000mm 29AWG cable, RA-RA vs. STR-STR



IL @ 16GHz	
Swift_RA_1m	-5.83 dB
Swift_STR_1m	-5.98 dB



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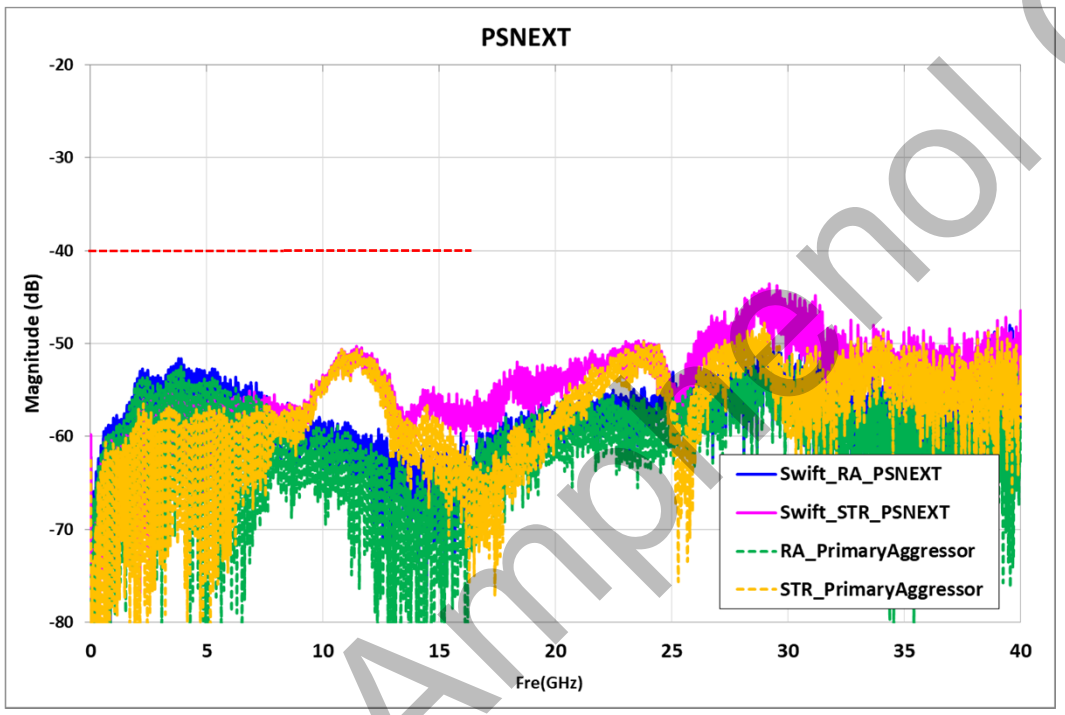
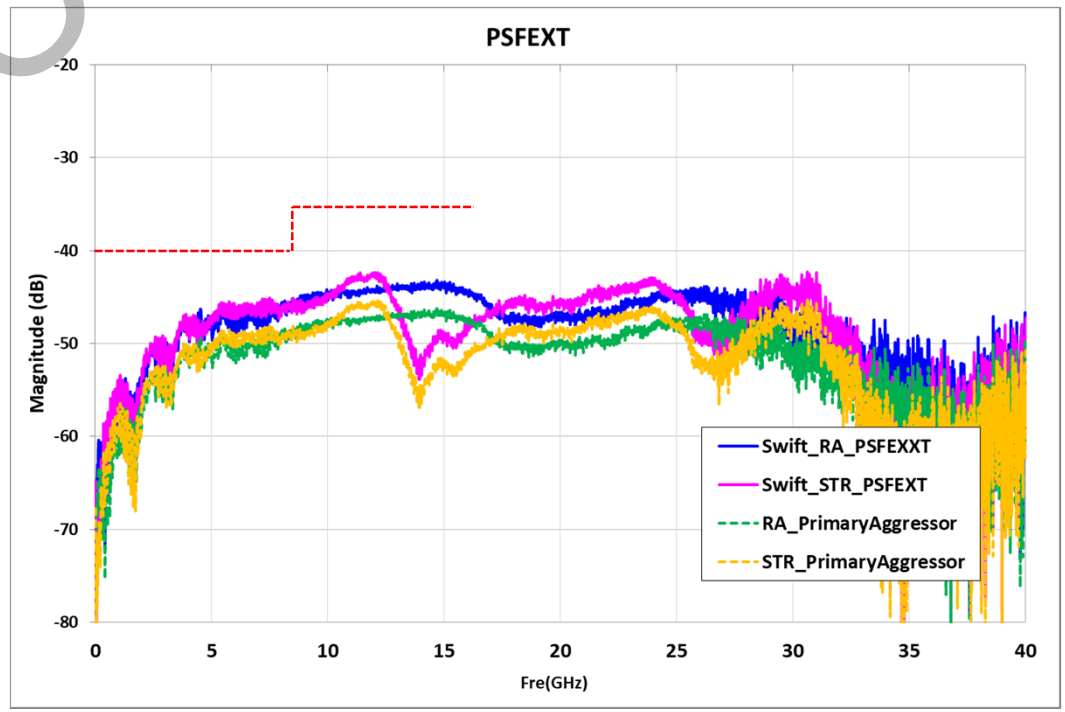
Swift & Swift DE_PCIe Gen5

G	G
TX0-	RX0-
TX0+	RX0+
G	G
TX1-	RX1-
TX1+	RX1+
G	G
TX2-	RX2-
TX2+	RX2+
G	G

G	G
RX0-’	TX0-’
RX0+’	TX0+’
G	G
RX1-’	TX1-’
RX1+’	TX1+’
G	G
RX2-’	TX2-’
RX2+’	TX2+’
G	G





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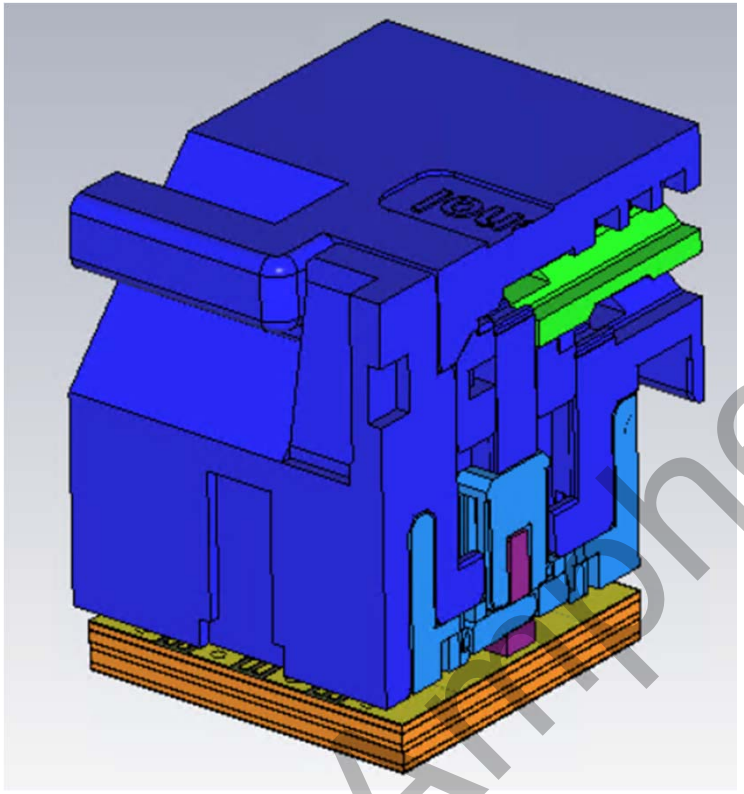
Benefits of SI

IL	Typical IL -6dB @ 16GHz (1000mm)
Crosstalk	Typical NEXT is -50dB, FEXT is -45dB @ 16GHz
Impedance	Supports 85ohm±10%(RT=15ps)

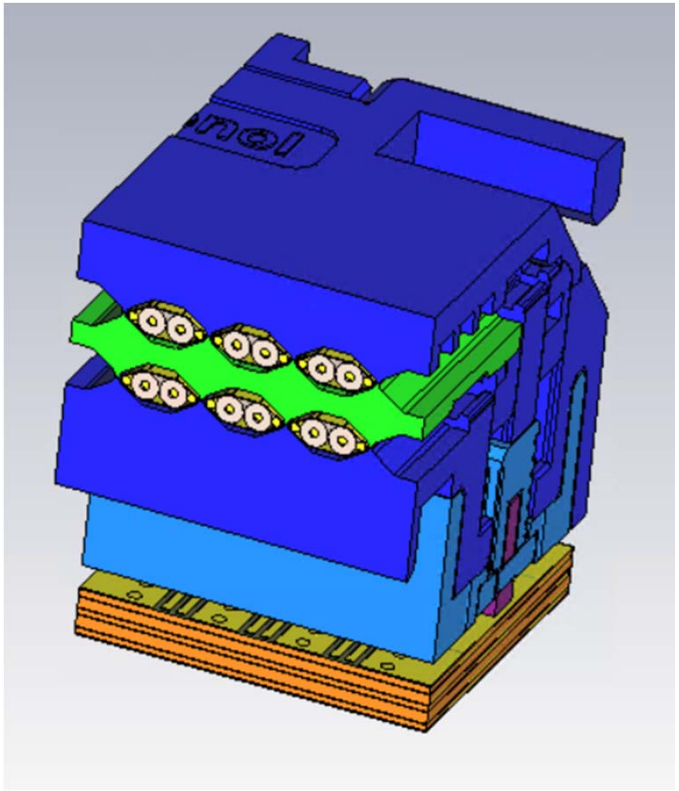
Swift & Swift DE_PCIe Gen6

SI simulation data is based on improved Swift RA plug with V/T receptacle. 1000mm 29AWG raw cable is used to cascaded into cable assembly.

AST proposed PCIe Gen6 cable spec (1000mm) is used.



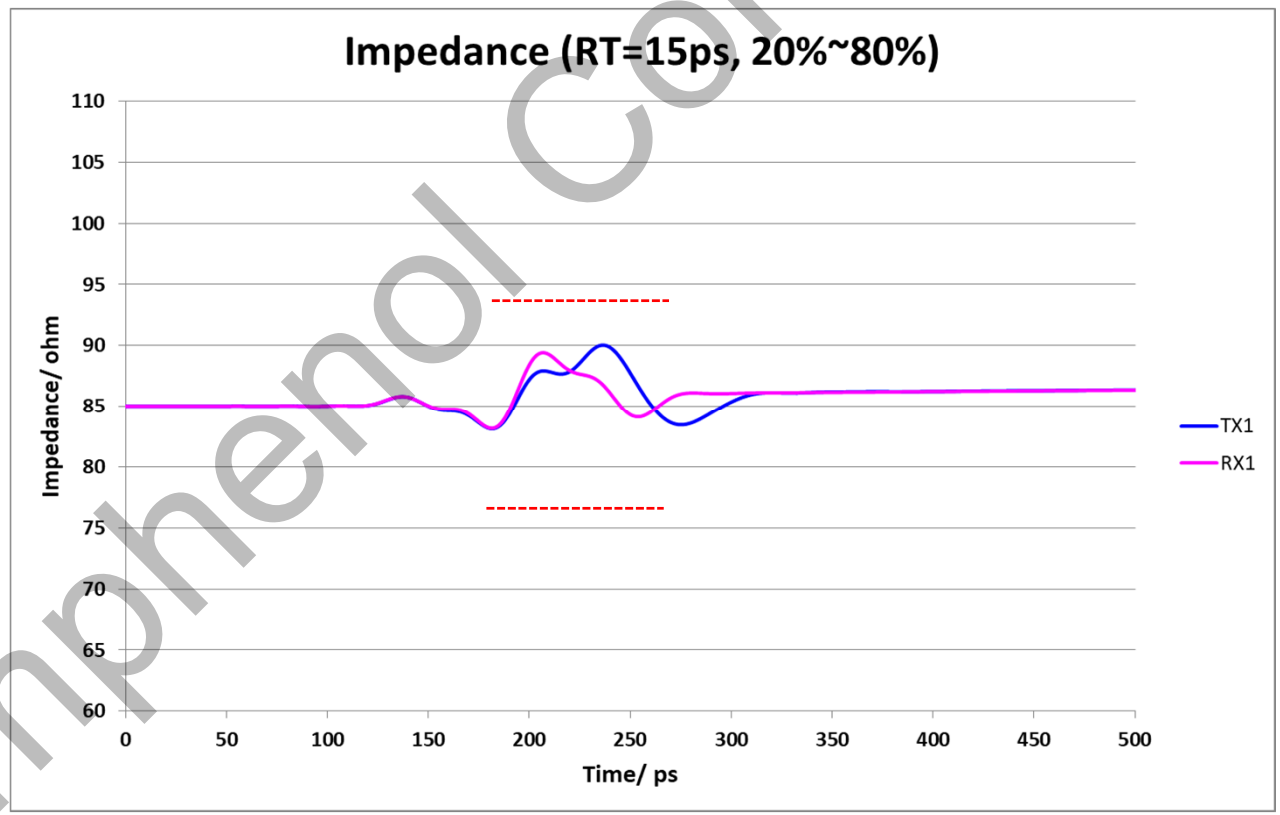
1M 29AWG Raw Wire



Swift & Swift DE_PCIe Gen6

SI simulation data is based on improved Swift RA plug with V/T receptacle. 1000mm 29AWG raw cable is used to cascaded into cable assembly.

AST proposed PCIe Gen6 cable spec (1000mm) is used.



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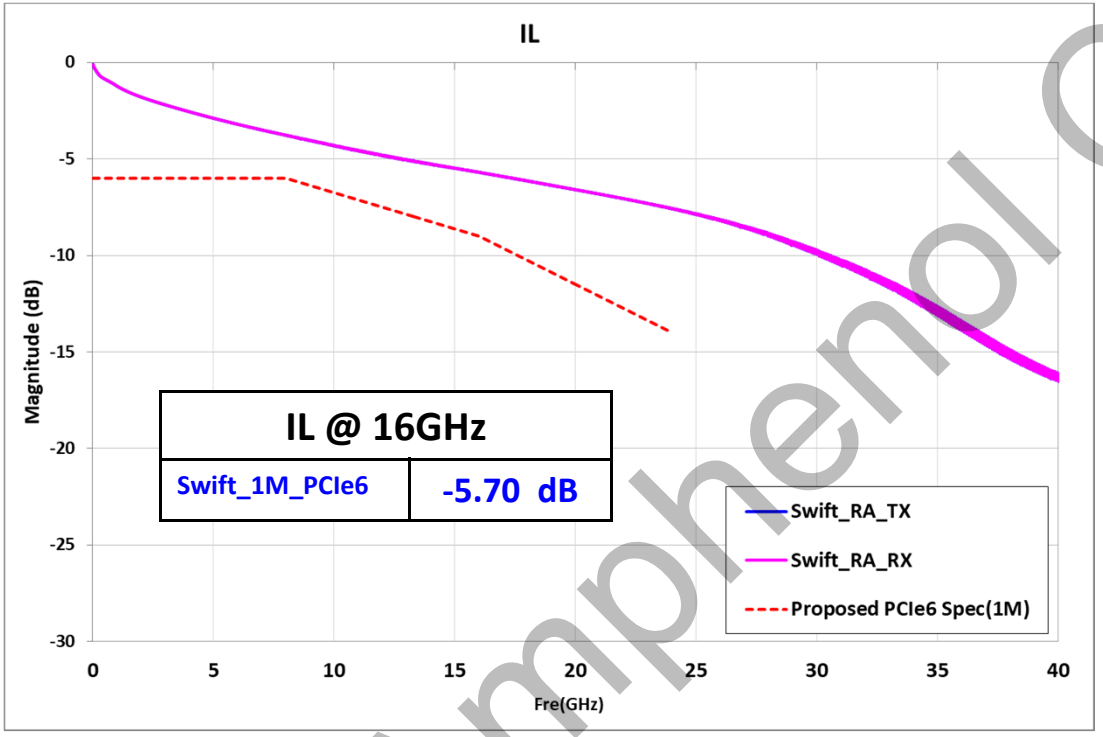
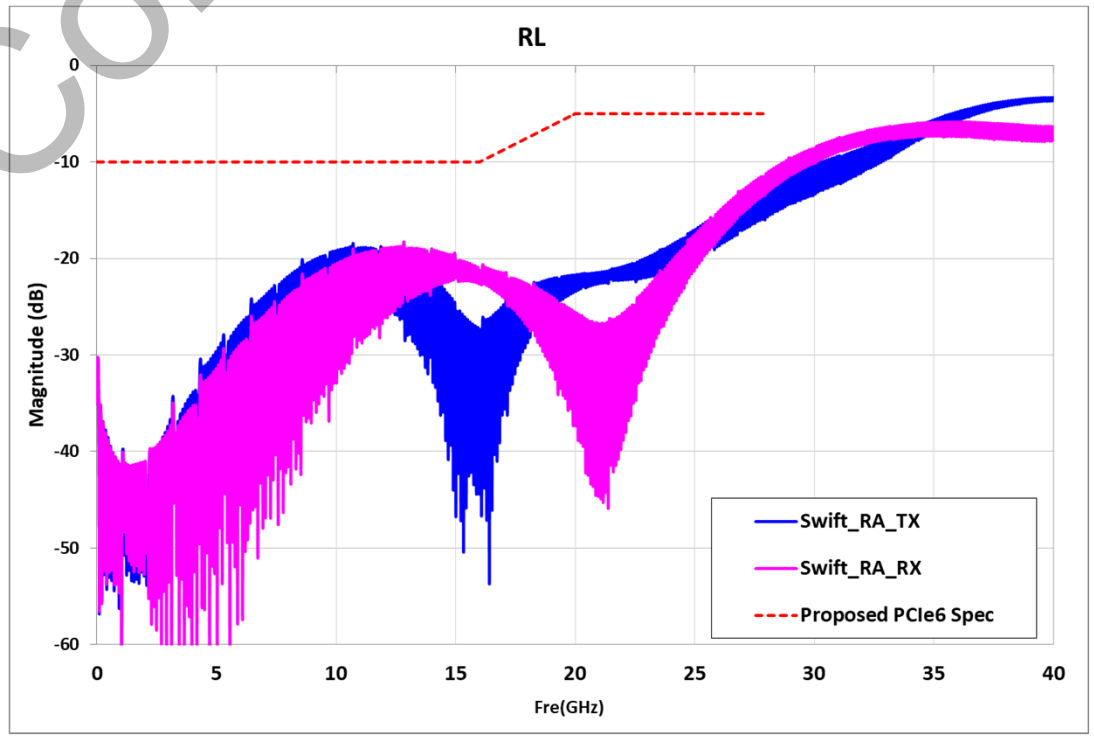
Swift & Swift DE_PCIe Gen6

SI simulation data is based on improved Swift RA plug with V/T receptacle. 1000mm 30AWG raw cable is used to cascaded into cable assembly.

AST proposed PCIe Gen6 cable spec (1000mm) is used.





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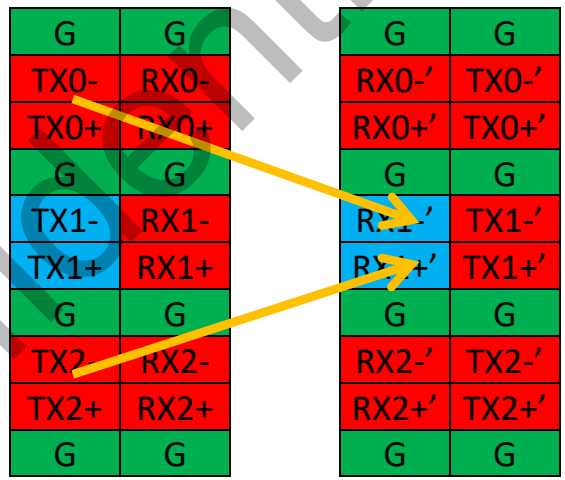
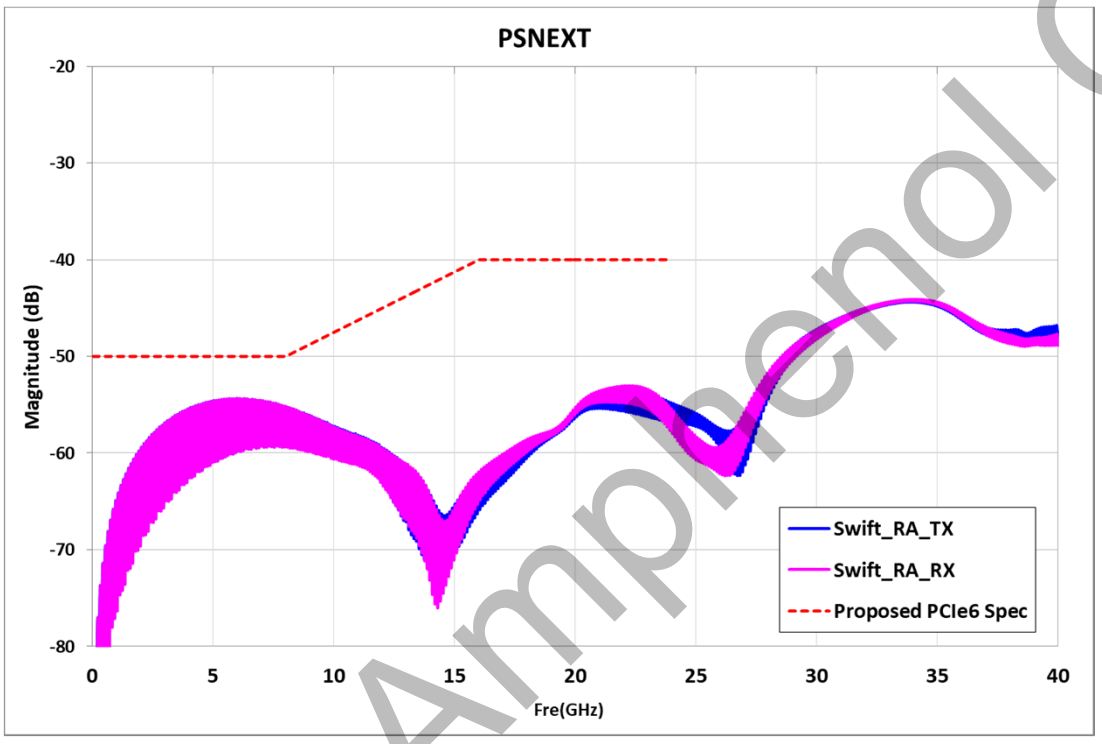
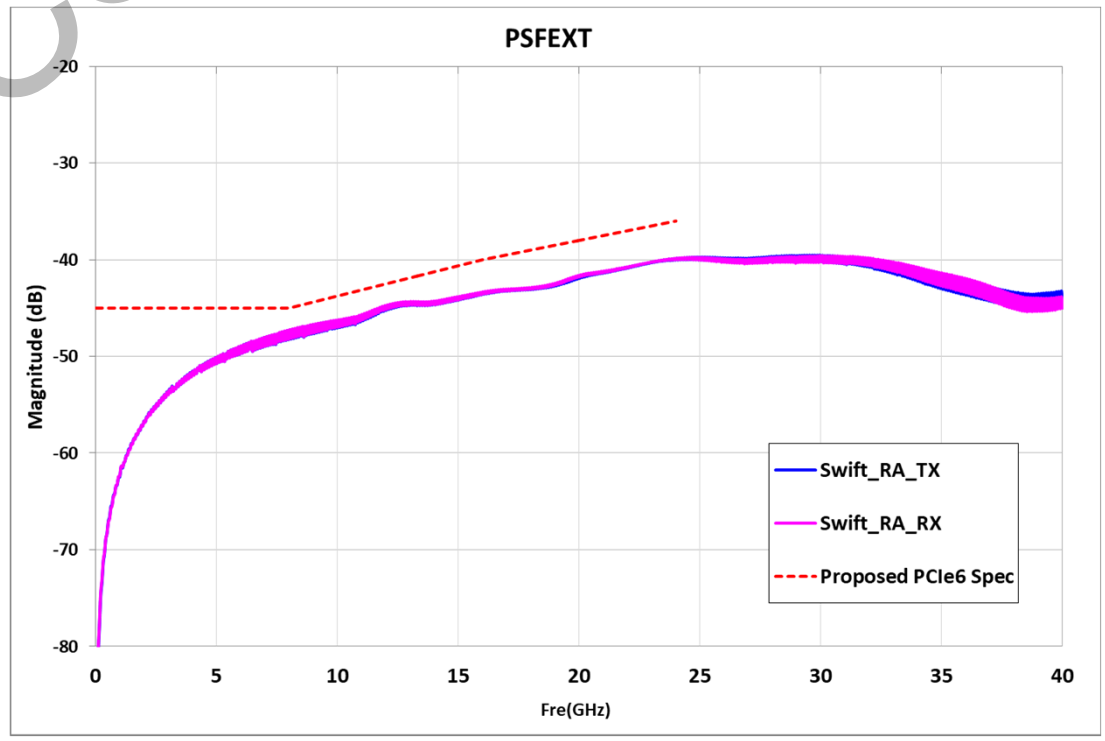
Swift & Swift DE_PCIe Gen6

G	G
TX0-	RX0-
TX0+	RX0+
G	G
TX1-	RX1-
TX1+	RX1+
G	G
TX2-	RX2-
TX2+	RX2+
G	G

G	G
RX0-’	TX0-’
RX0+’	TX0+’
G	G
RX1-’	TX1-’
RX1+’	TX1+’
G	G
RX2-’	TX2-’
RX2+’	TX2+’
G	G







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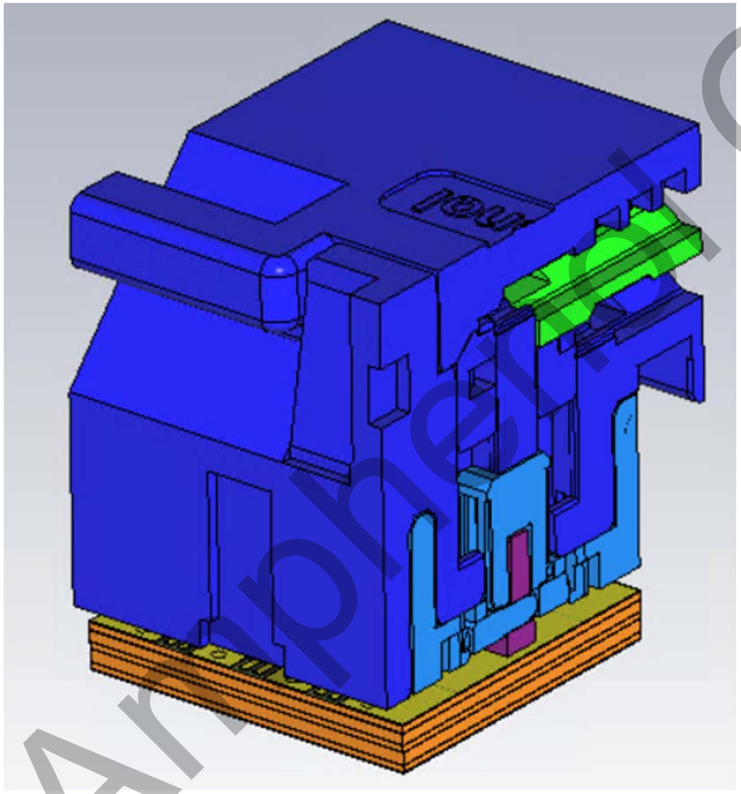
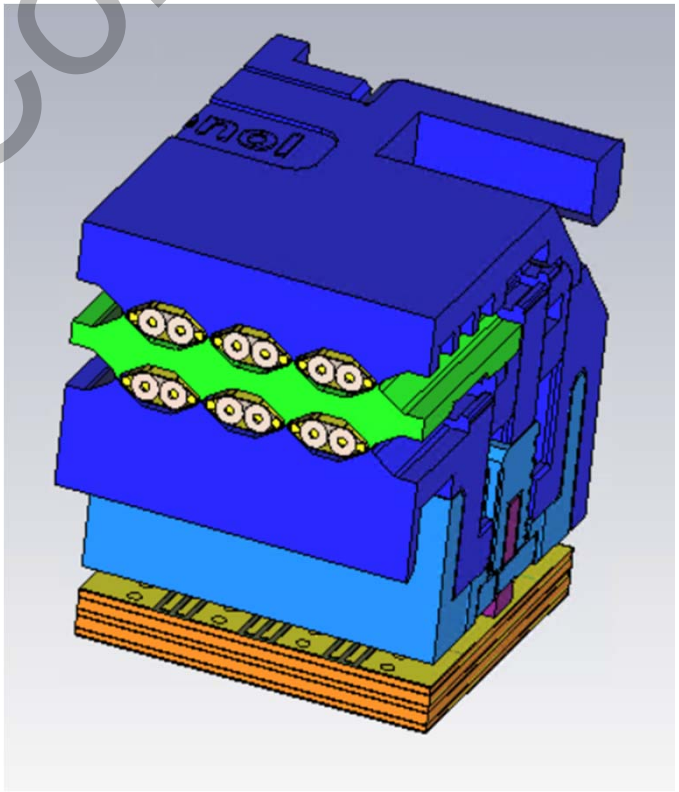
Swift & Swift DE_112G PAM4

SI simulation data is based on improved Swift RA plug with V/T receptacle, wire termination considered.

SFF-TA-1002 112G PAM4 spec used is for connector only.
(*Our model with termination considered still pass with good margin.)

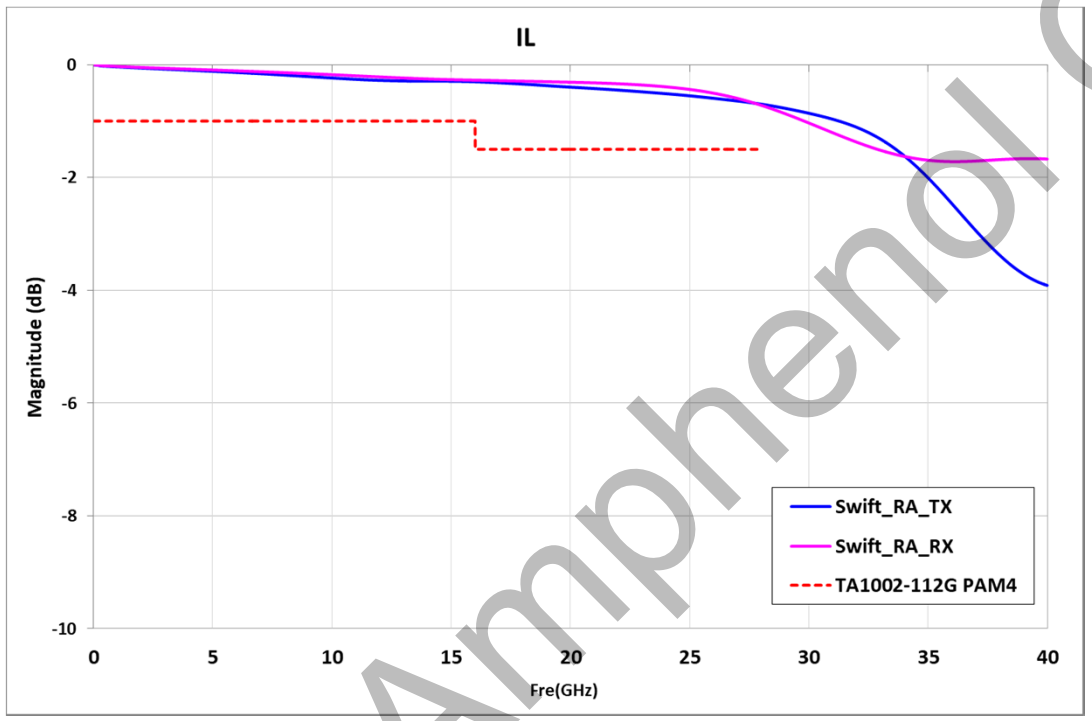


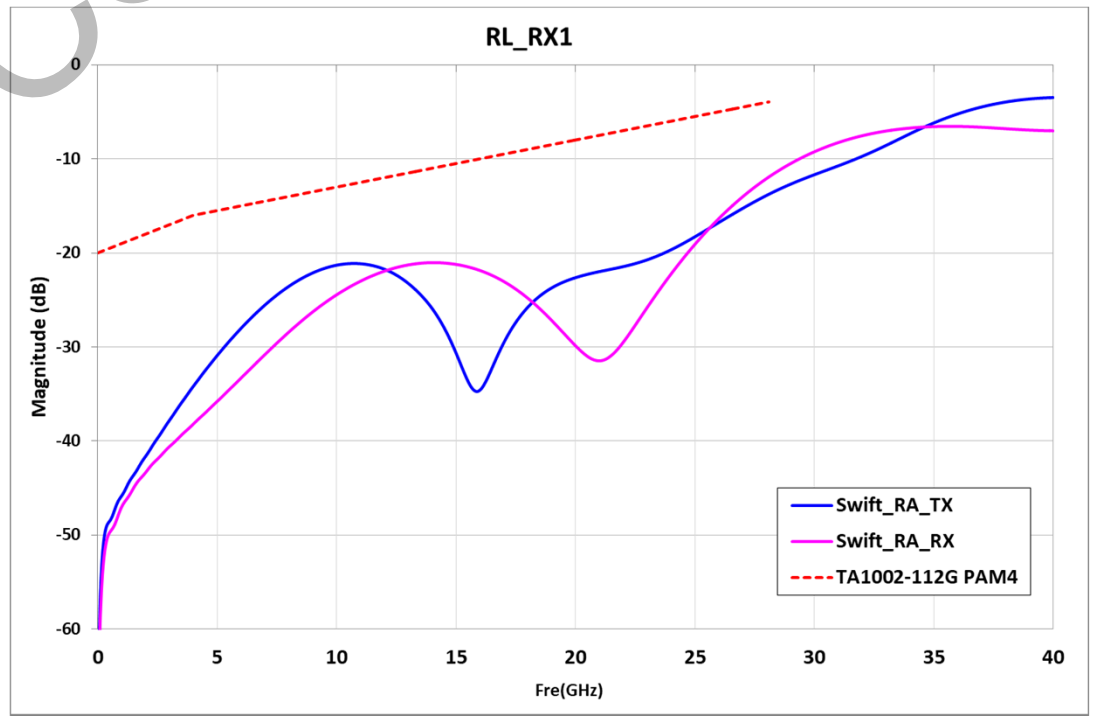


Swift & Swift DE_112G PAM4

SI simulation data is based on improved Swift RA plug with V/T receptacle, wire termination considered.

SFF-TA-1002 112G PAM4 spec used is for connector only.
(*Our model with termination considered still pass with good margin.)





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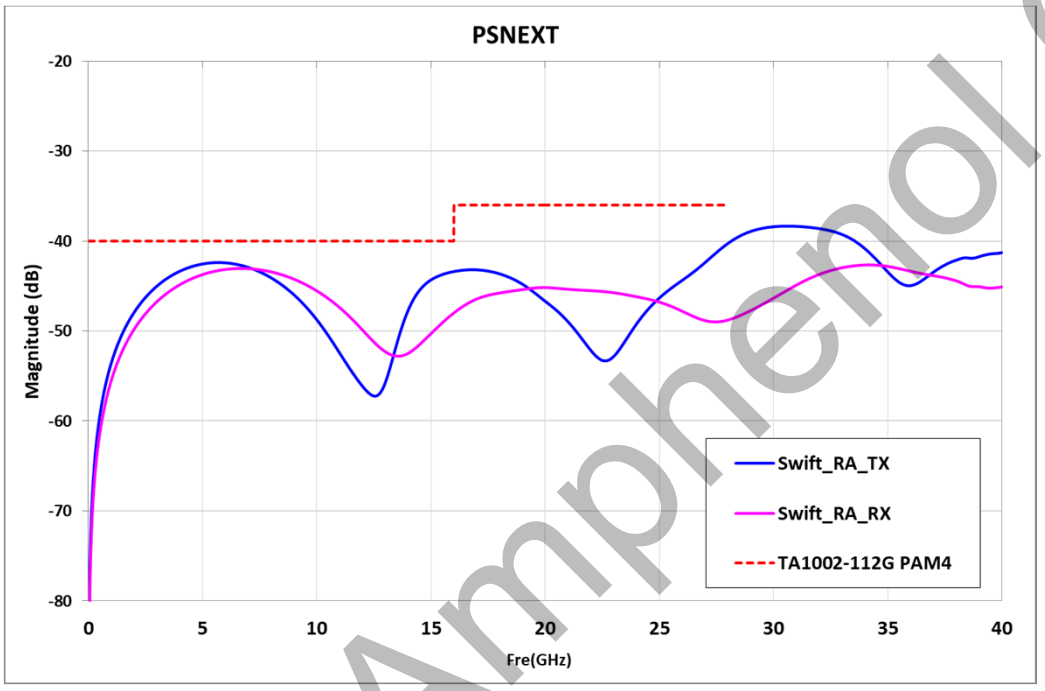
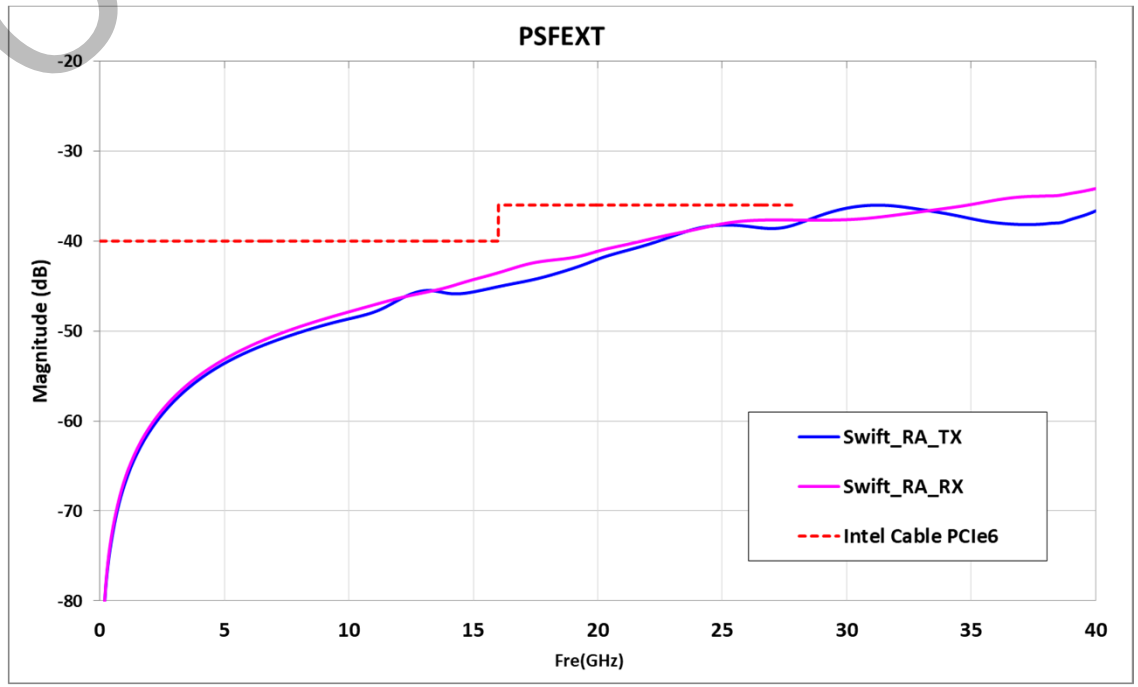
Swift & Swift DE_112G PAM4





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Riser Card "ODC" Cable Solution

On Demand Connector

Riser Card ODC Cable Solution

ODC solution is designed to bring the connector to the solder joint termination and can be customized to the application. It supports PCIe Gen5 and is scalable to GEN 6. It allows for more stability in impedance and IL at the twin-ax solder joint.

SI

- Supports proposed PCIe Gen5 standard
- ODC design improved IL and impedance

Mechanical

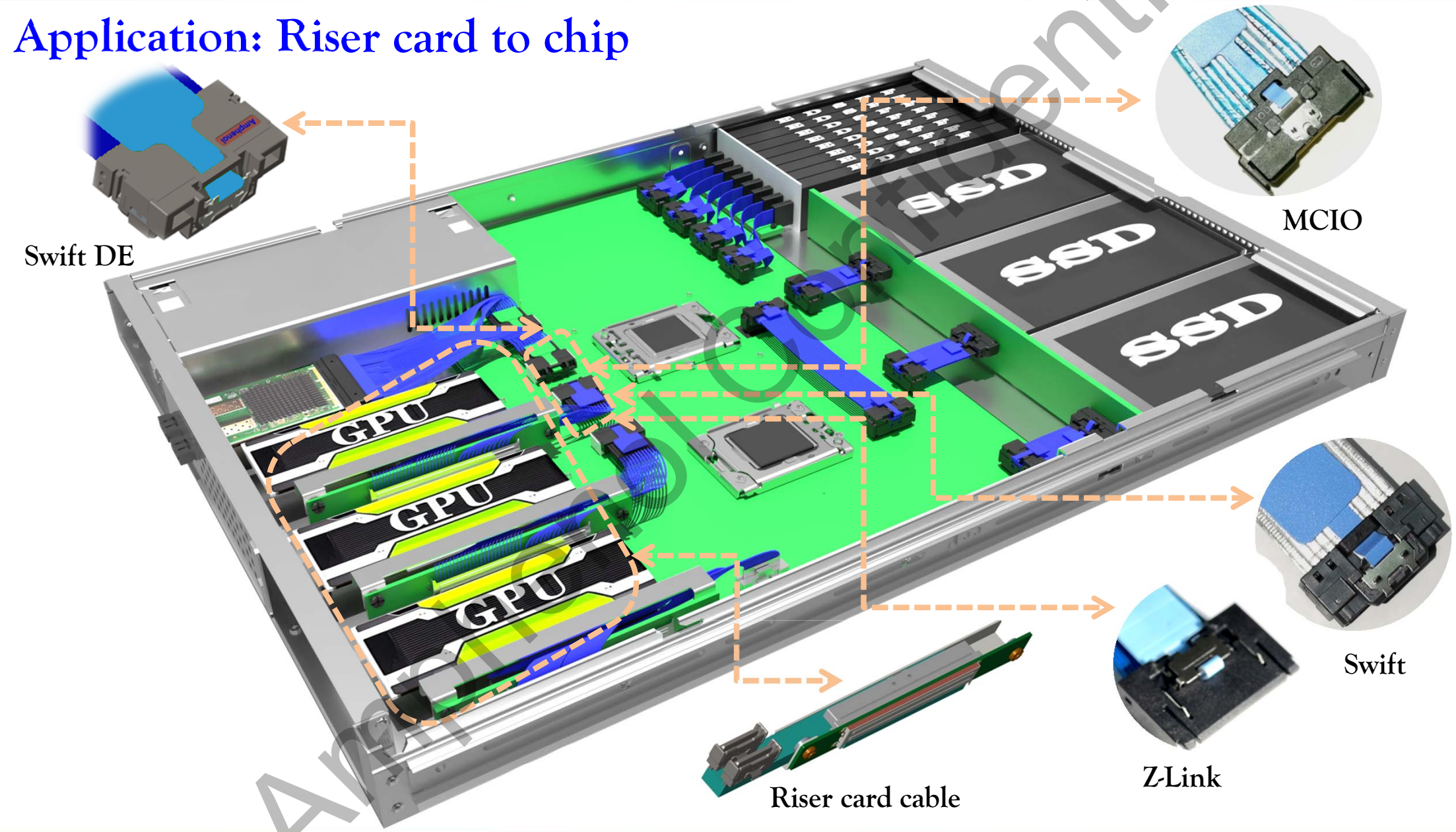
- Metal shell protects solder joint and improves stress-strain

Application

- Riser card PCBA can be customized to the application

Riser Card ODC Cable Solution

Application: Riser card to chip



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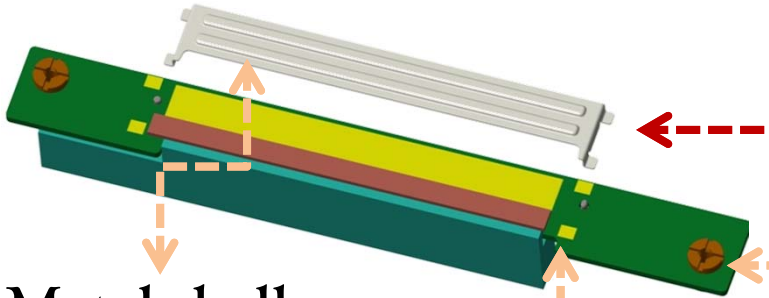
Riser Card ODC Cable Solution

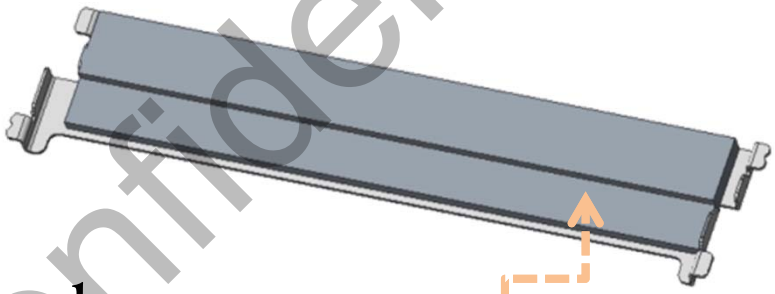
Mechanical: Features of ODC assembly



Metal shell

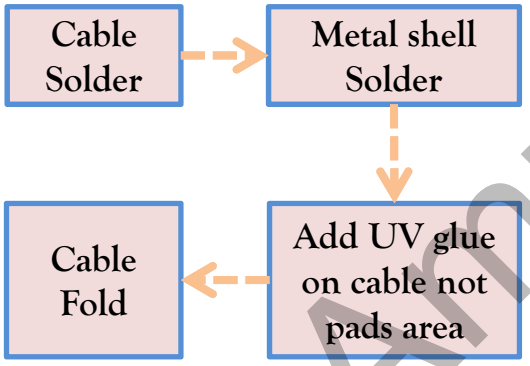
Solder pads
for metal shell

Customized
PCIe PCBA



Bottom face: foam tape
stick on metal shell

Process flow chart:



UV glue on cable

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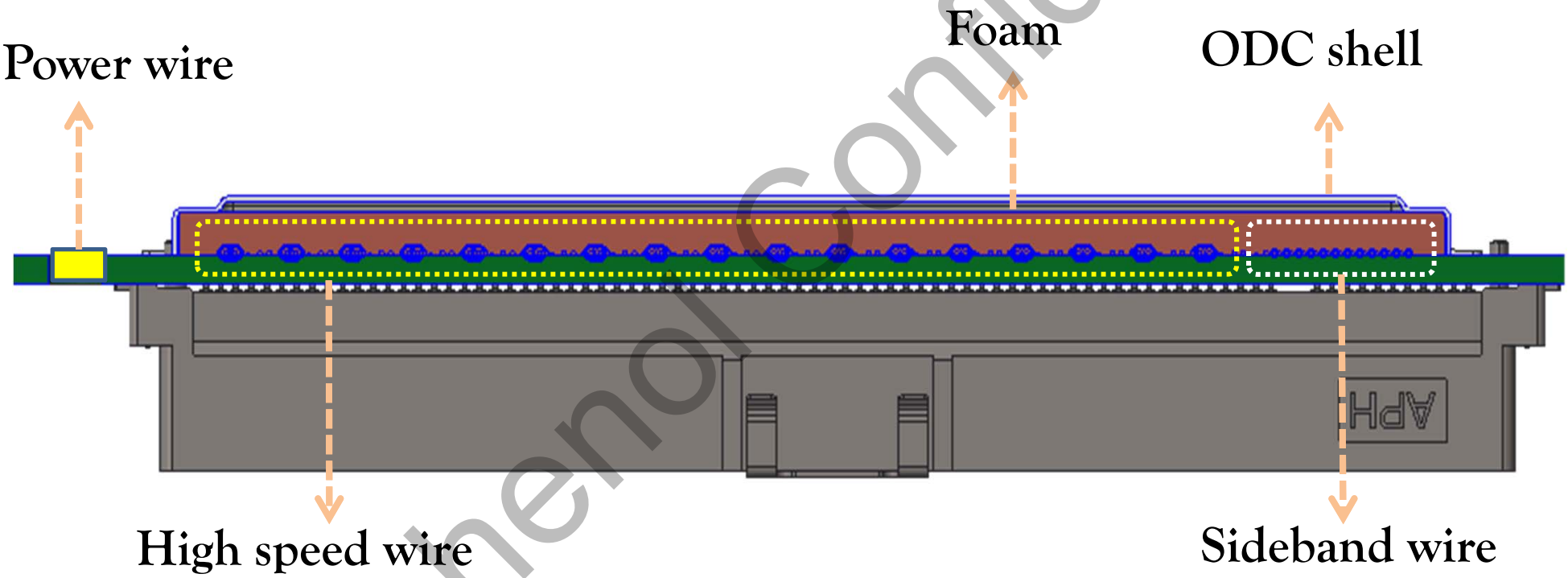
Riser Card ODC Cable Solution

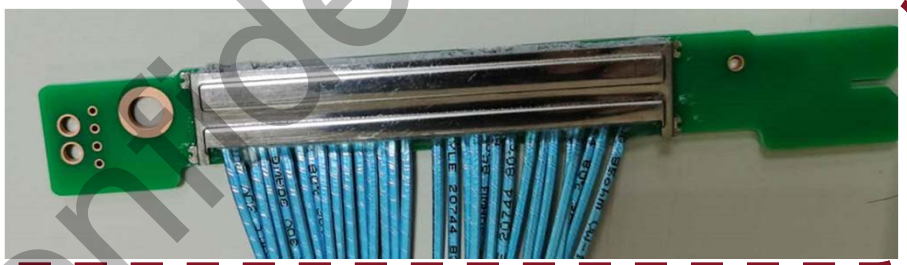
Mechanical: Cross section

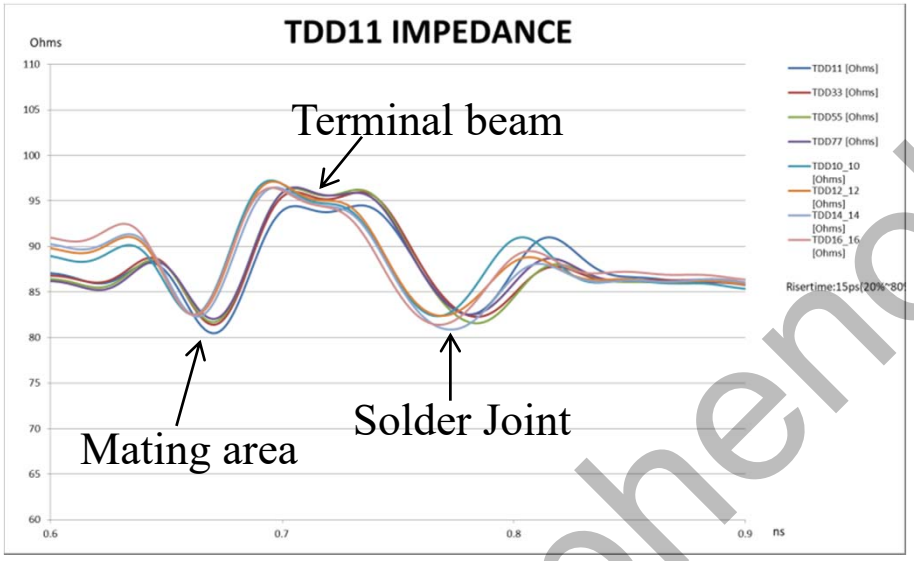


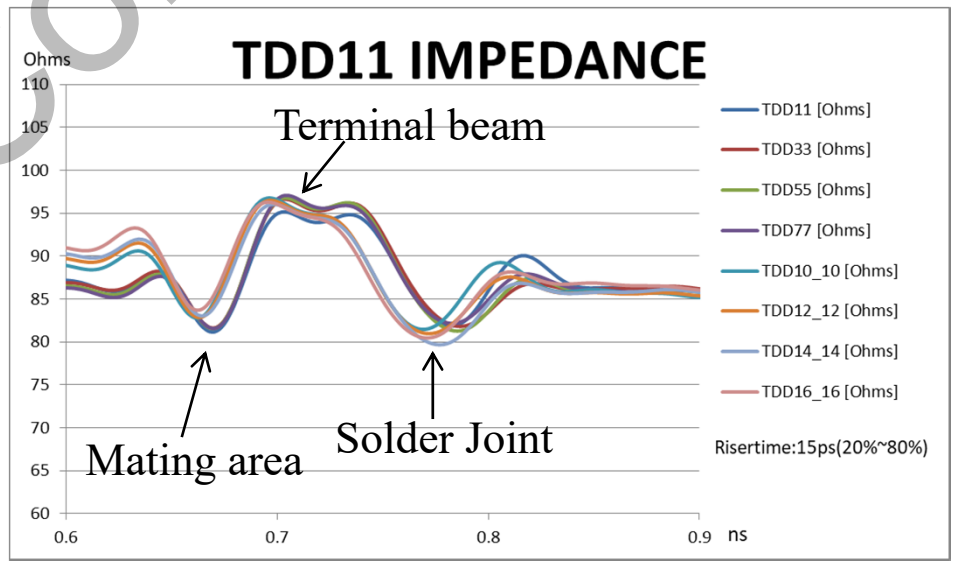
Foam material: EFOAM is a shock absorbing, highly damped material

Riser Card ODC Cable Solution

Mechanical: TDR response before and after cover installation







Approximate changed in impedance from 80ohm to 81ohm.

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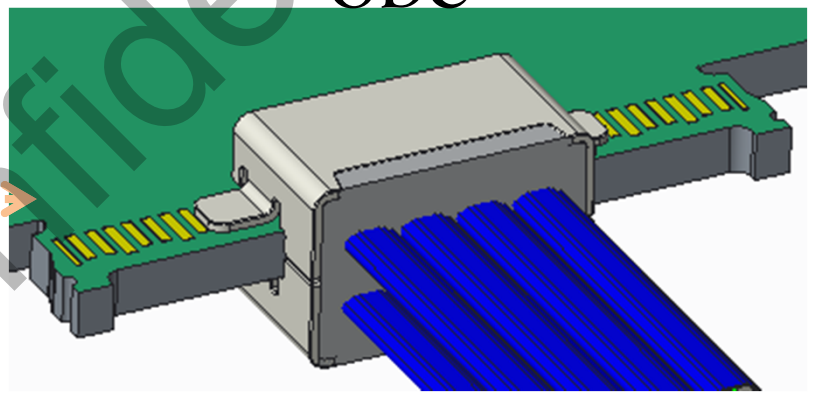
Riser Card ODC Cable Solution

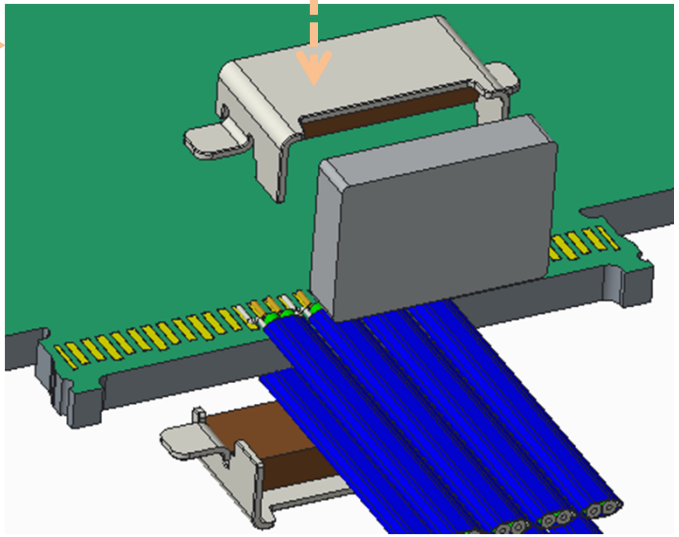
SI test board & ODC characterization
AFR calibration for IL only

3D is for illustration Reference

ODC



Metal shell with foam



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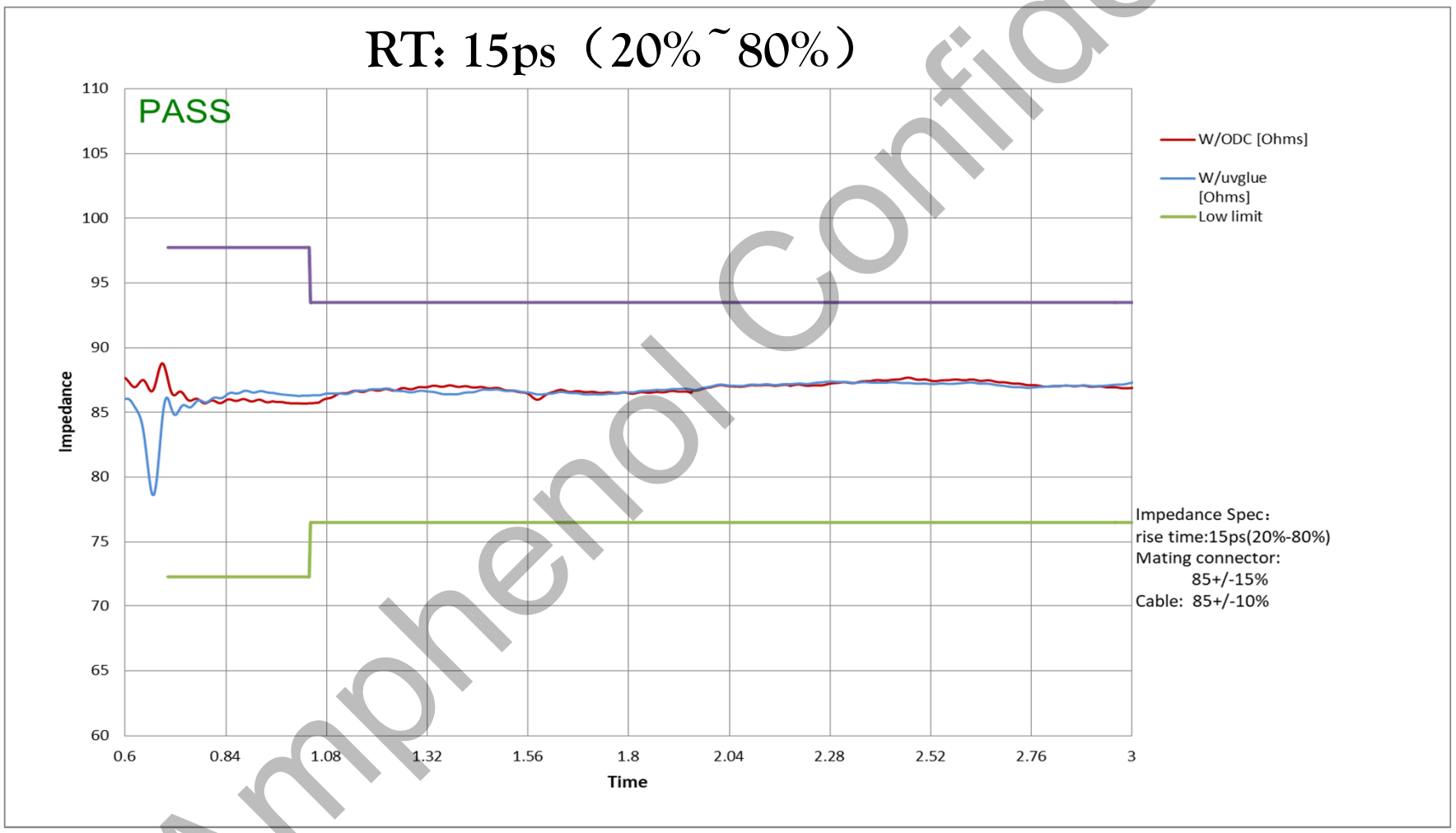
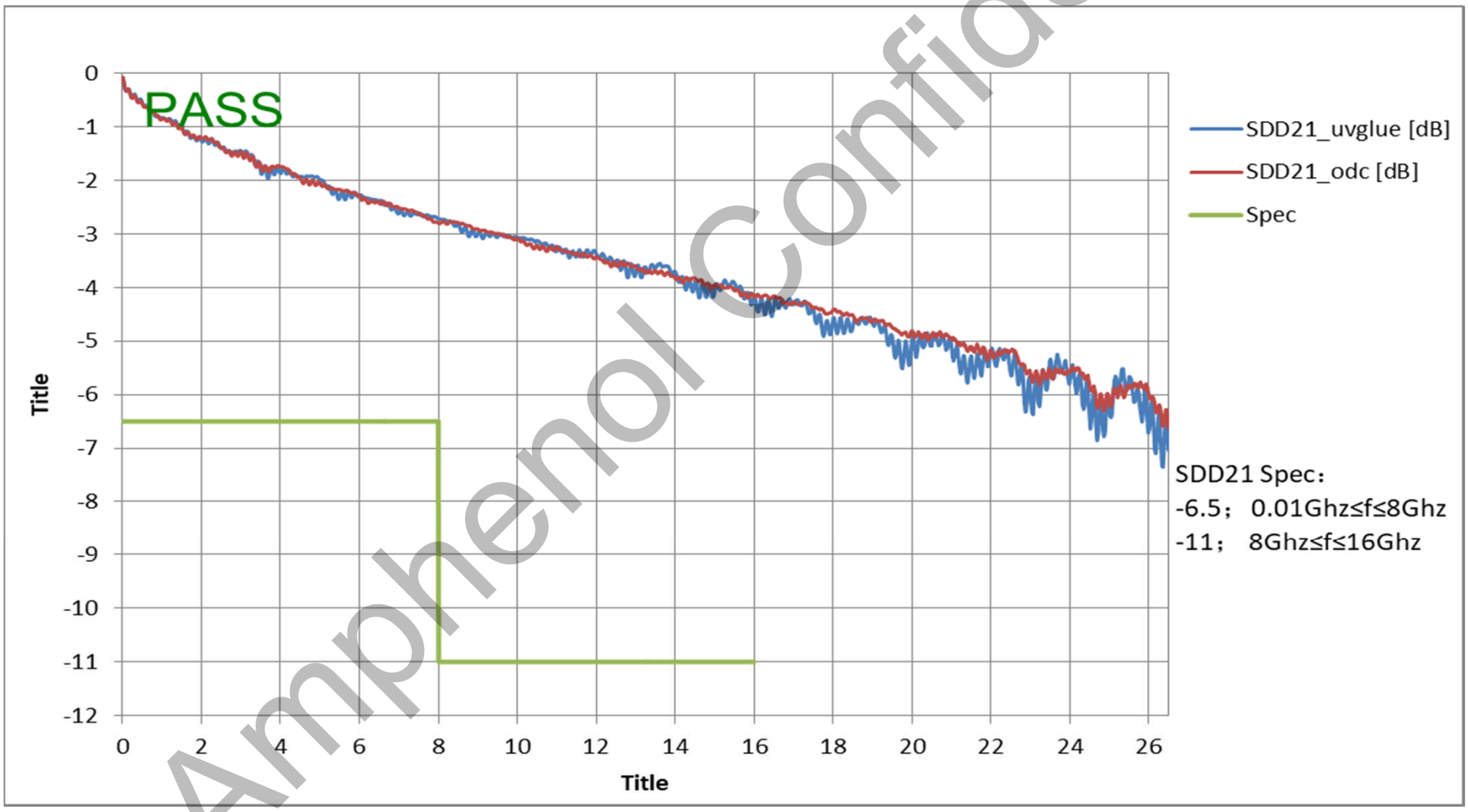
Riser Card ODC Cable Solution

Impedance(measured): ODC T-Shape test board with 29AWG 600mm raw cable UV glue VS. ODC



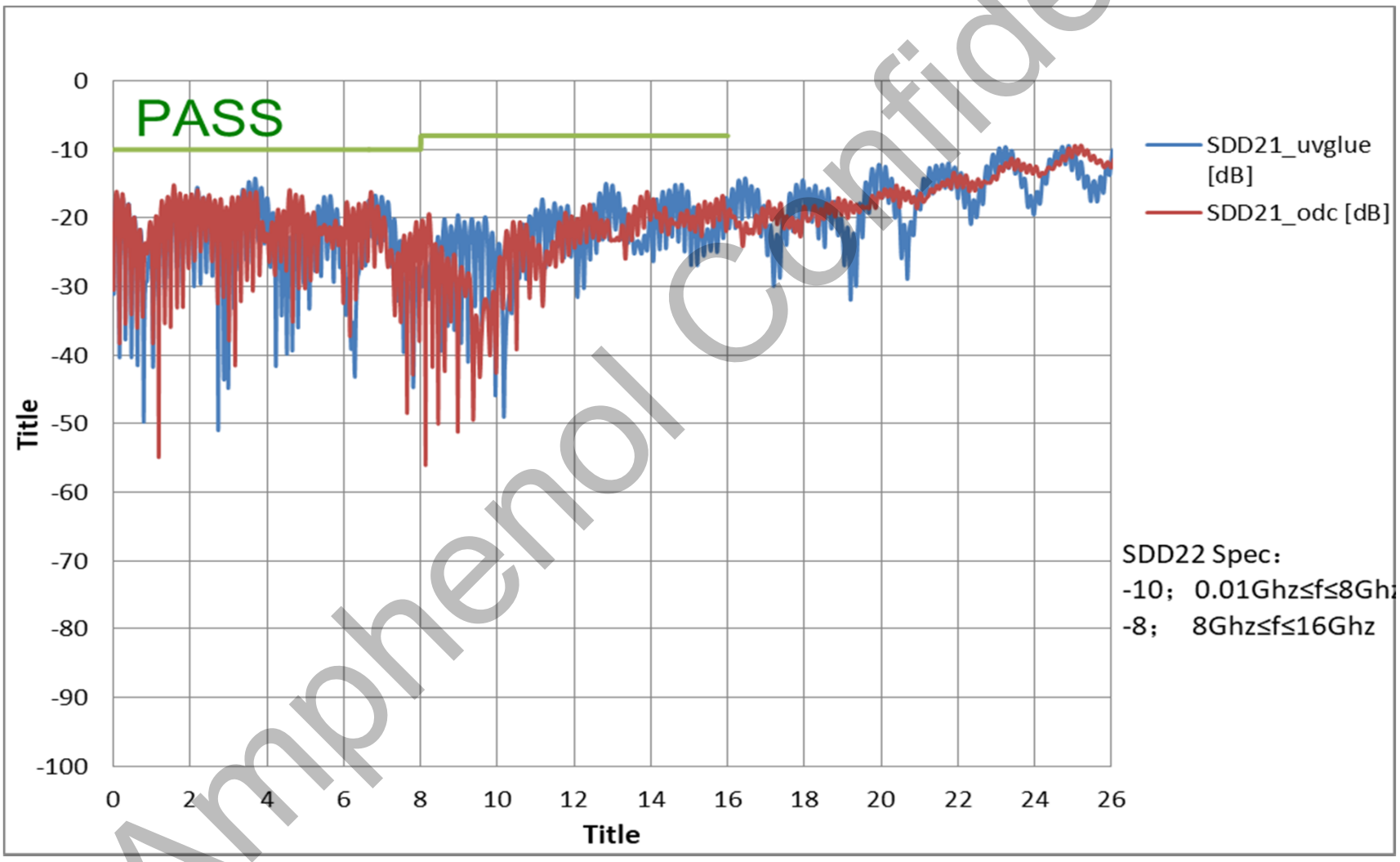
Riser Card ODC Cable Solution

IL(measured): ODC T-Shape test board with 29AWG 600mm raw cable UV glue VS. ODC



Riser Card ODC Cable Solution

RL (measured): ODC T-Shape test board with 29AWG 600mm raw cable UV glue VS. ODC



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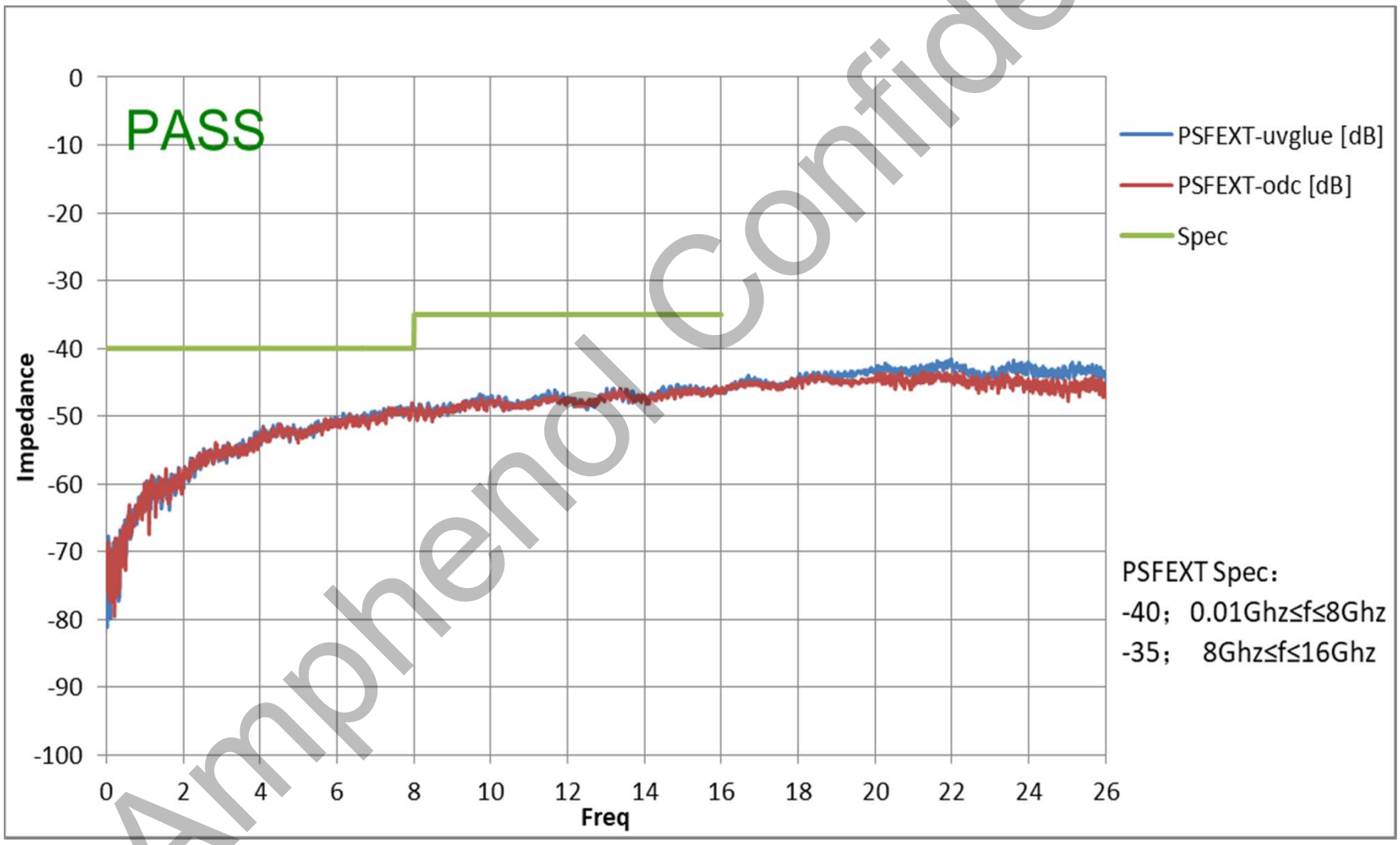
Riser Card ODC Cable Solution

FEXT(measured): ODC T-Shape test board with 29AWG 600mm raw cable UV glue VS. ODC



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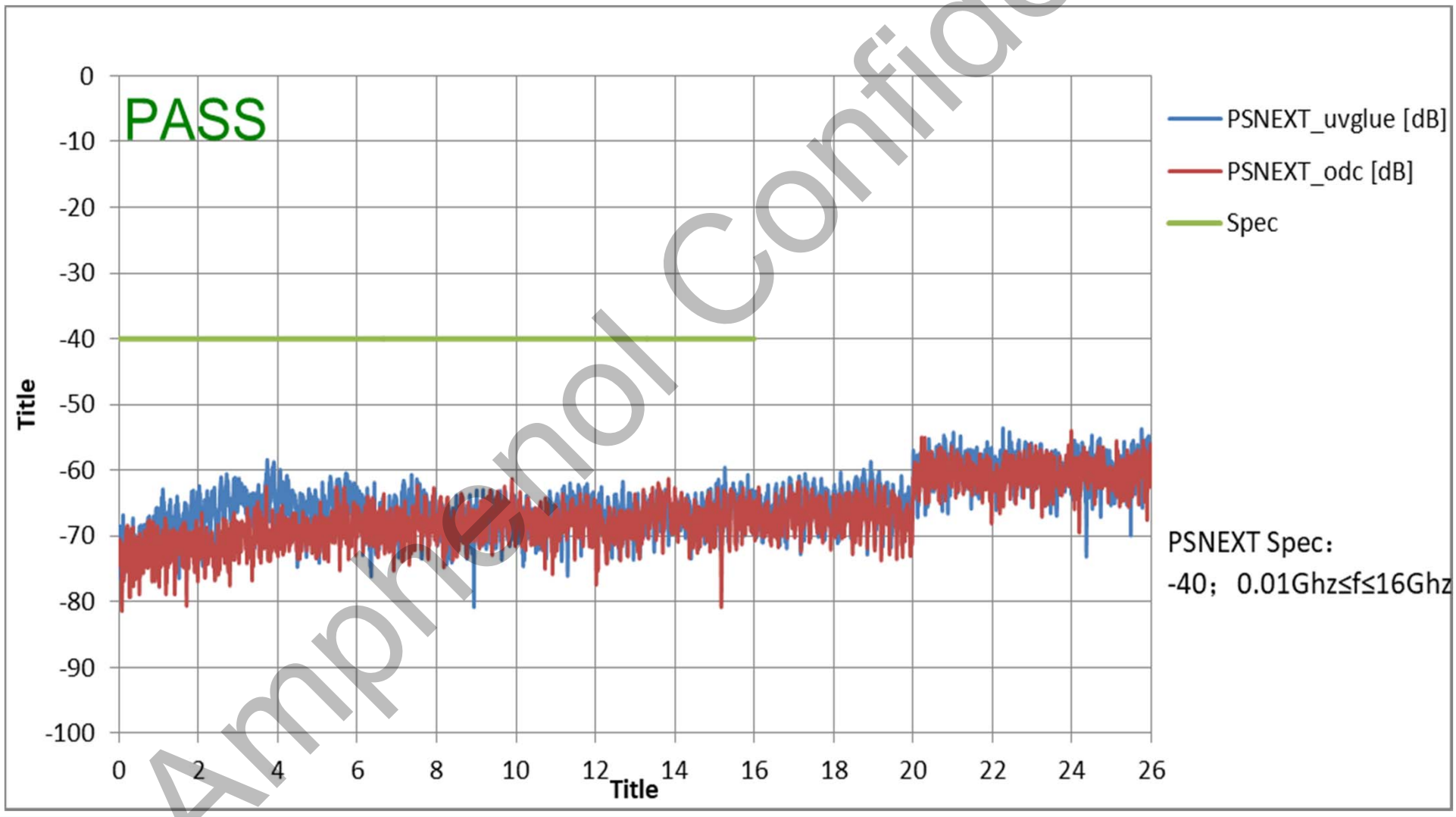
Riser Card ODC Cable Solution

NEXT(measured): ODC T-Shape test board with 29AWG 600mm raw cable UV glue VS. ODC



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Riser Card ODC Cable Solution

W/ UV glue design

Pros

Reduce height

Cost effective

Cons

Impedance tendency to dip lower and IL tends to slightly ring more.

W/ ODC design

Pros

Support proposed PCIe Gen5 and PCIe Gen6

Optimized cable routing

Protect solder joint in narrow space

Cons

Cost higher than W/ UV glue design

Note: the cost evaluation was based on one ODC.

Riser Card ODC Cable Solution

Highlight

SI

- ODC improved cable IL and impedance of solder joint
- Supports proposed PCIe Gen5, scalable to support PCIe Gen6

Mechanical

- Metal shell protect solder joint

Application

- Customize to customer applications

Blind Mate

Blind Mate

Blind mate is a high-speed high density cable solution with primary and secondary guide features. The robust mechanical design with anti-reverse feature can reach data rates up to PCIe Gen5 and is scalable to reach PCIe Gen6.

SI

- Supports proposed PCIe Gen5 standard
- Scalable to support PCIe Gen6 standard

Mechanical

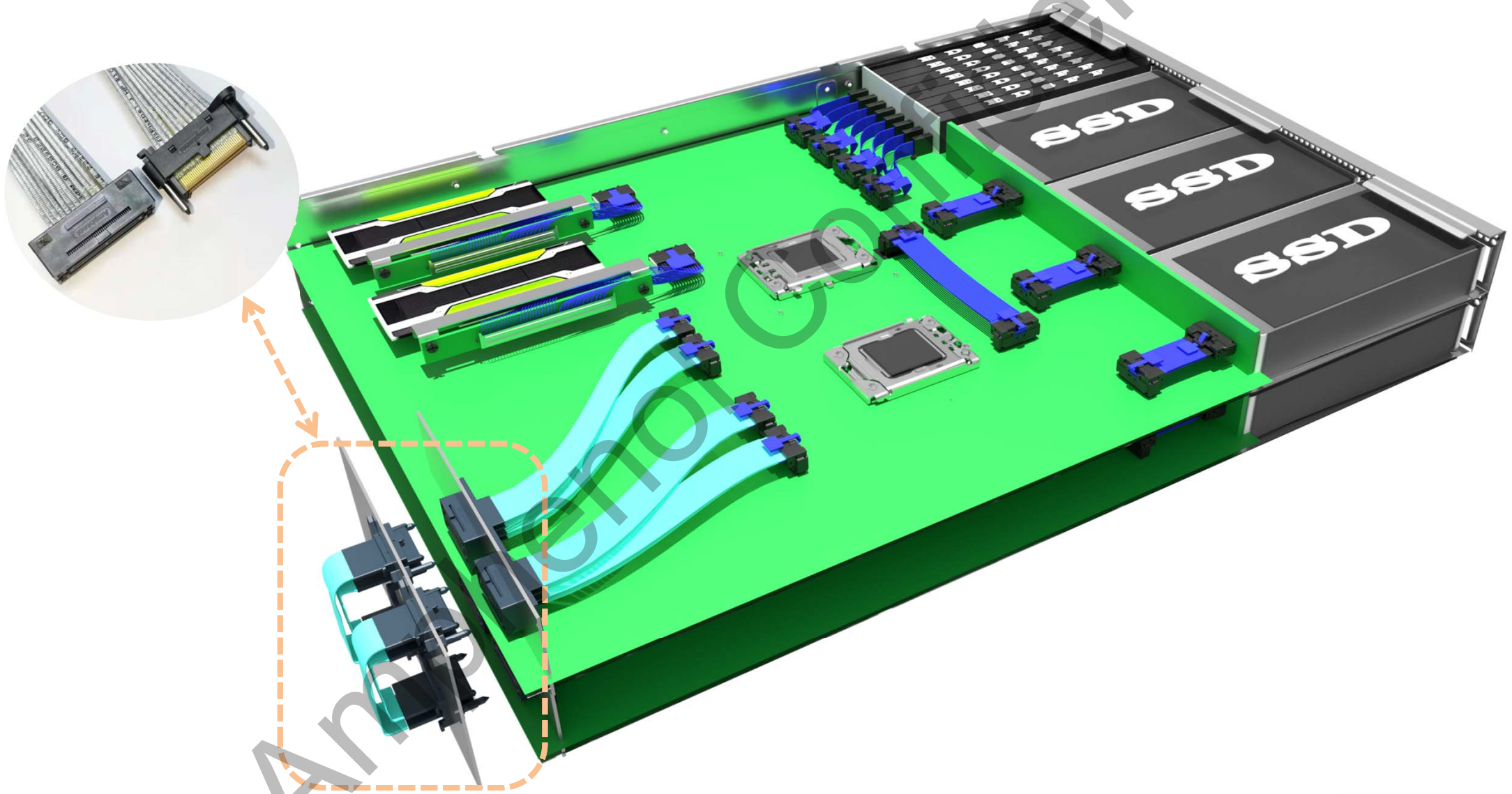
- Primary and secondary guide feature

Application

- Support UPI2.0 architecture and chip to backplane

Blind Mate

Application: High speed connection between multiple mother boards



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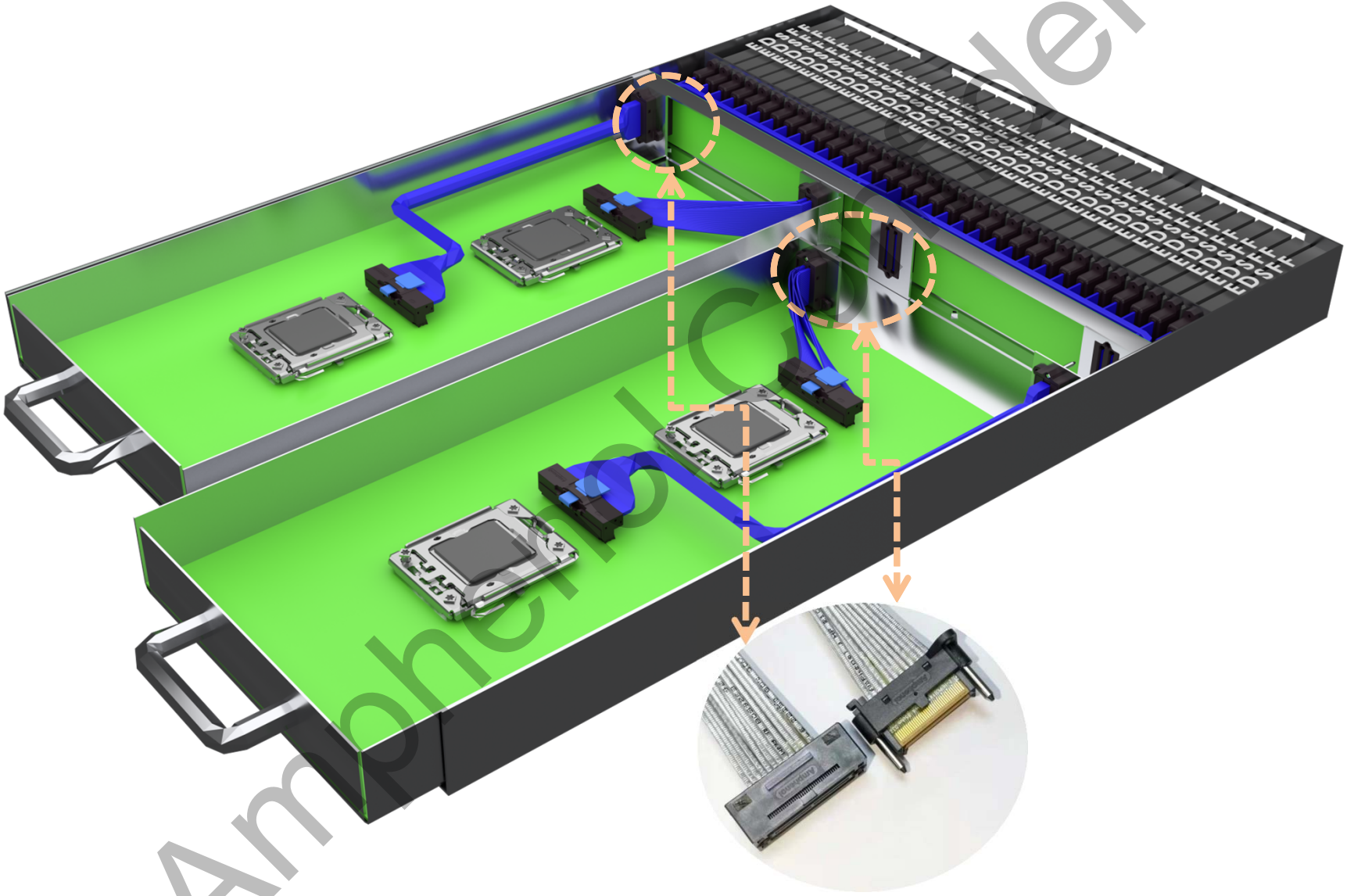
Blind Mate

Application: Chip to backplane



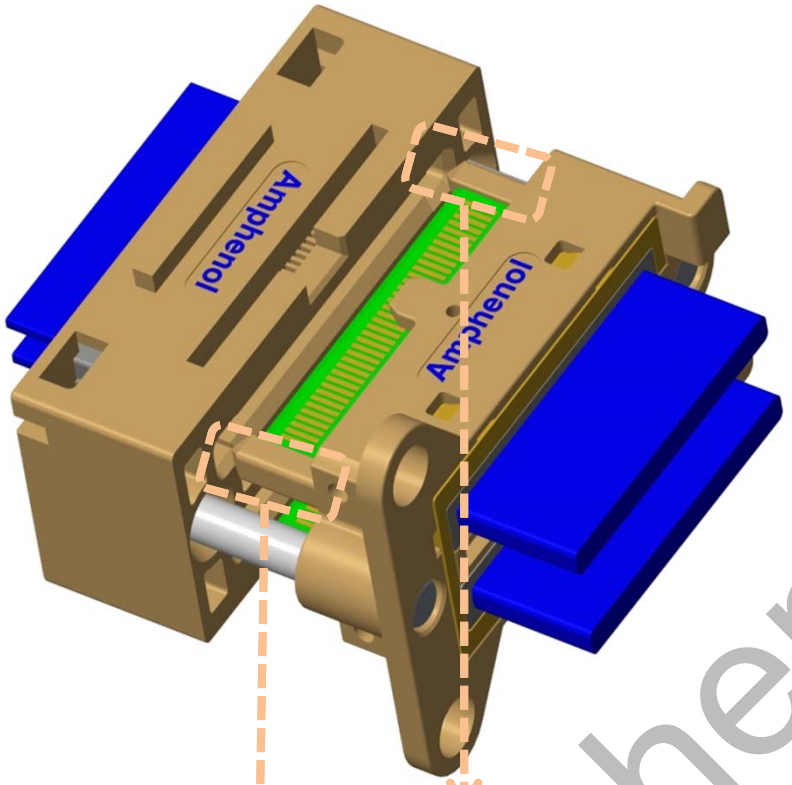
Blind Mate

Benefits of application

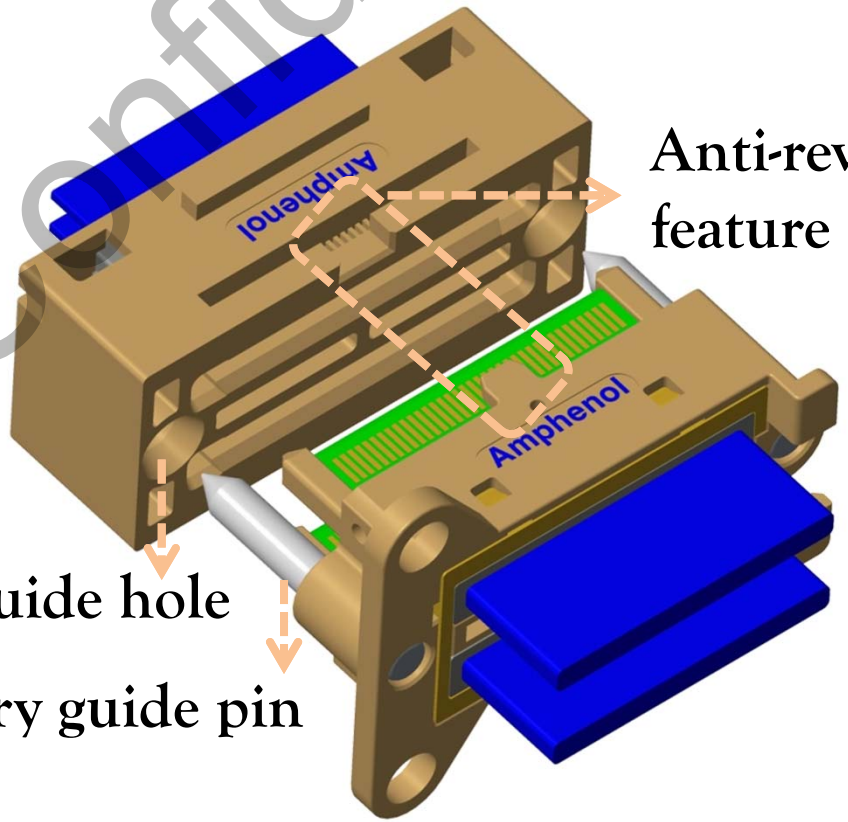
- **High speed**
  - Supports proposed PCIe Gen5 standard
  - Scalable to PCIe Gen6
- **Blind mate**
  - Allowable tolerance 1.5mm
- **Multiple applications**
  - Cable to cable, cable to board

Blind Mate

Mechanical: Primary and secondary guide feature



Secondary guide feature



Anti-reverse feature

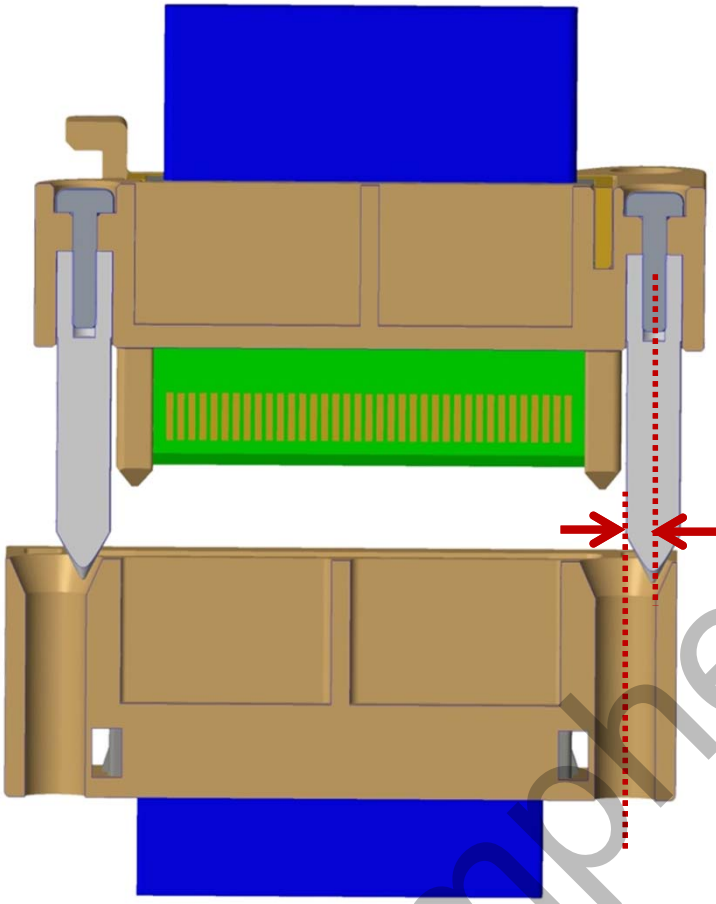
Guide hole

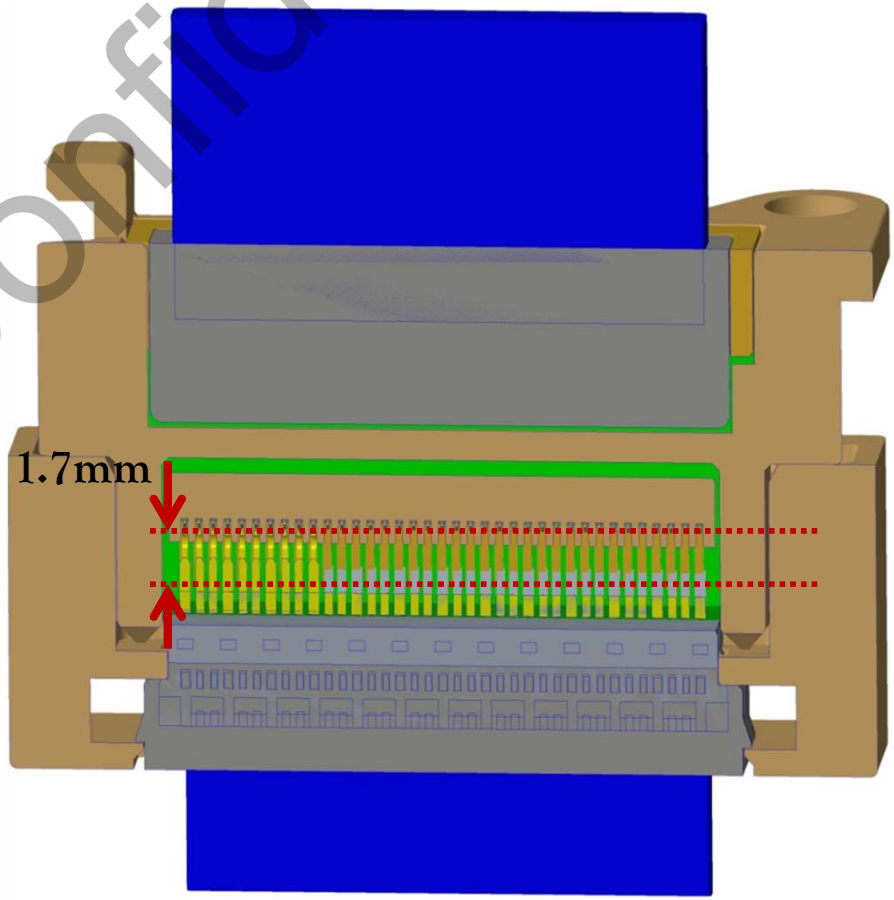
Primary guide pin

Amphenol

Blind Mate

Mechanical: Allowable tolerance1.5mm&wipe length is 1.7mm





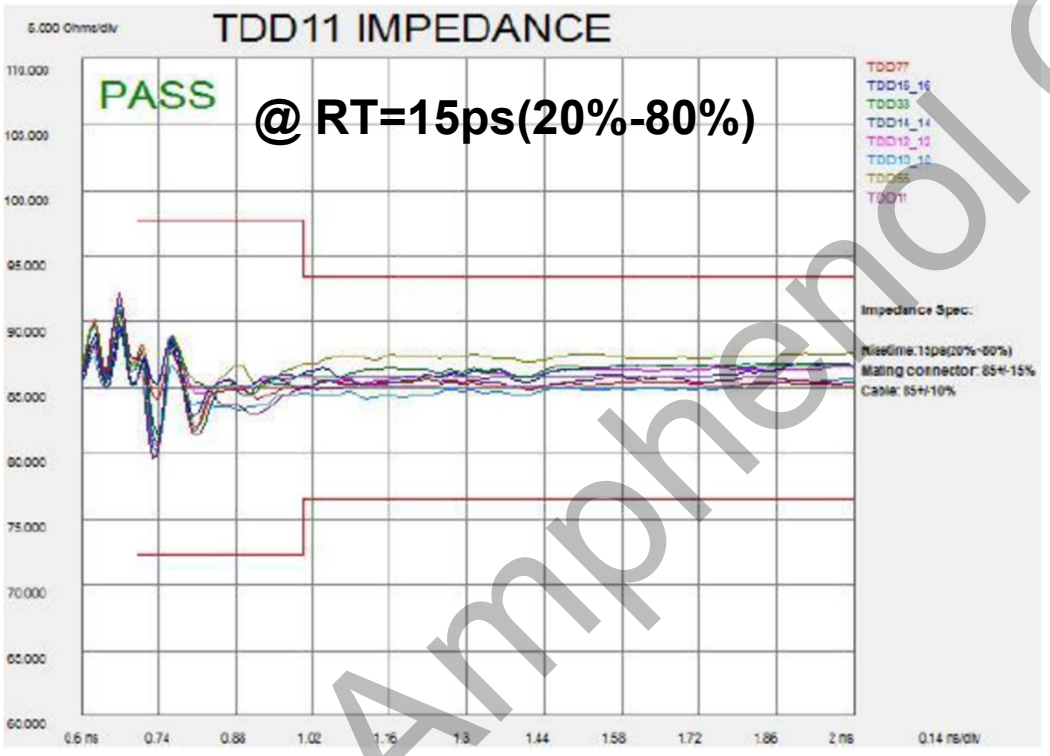
Blind Mate

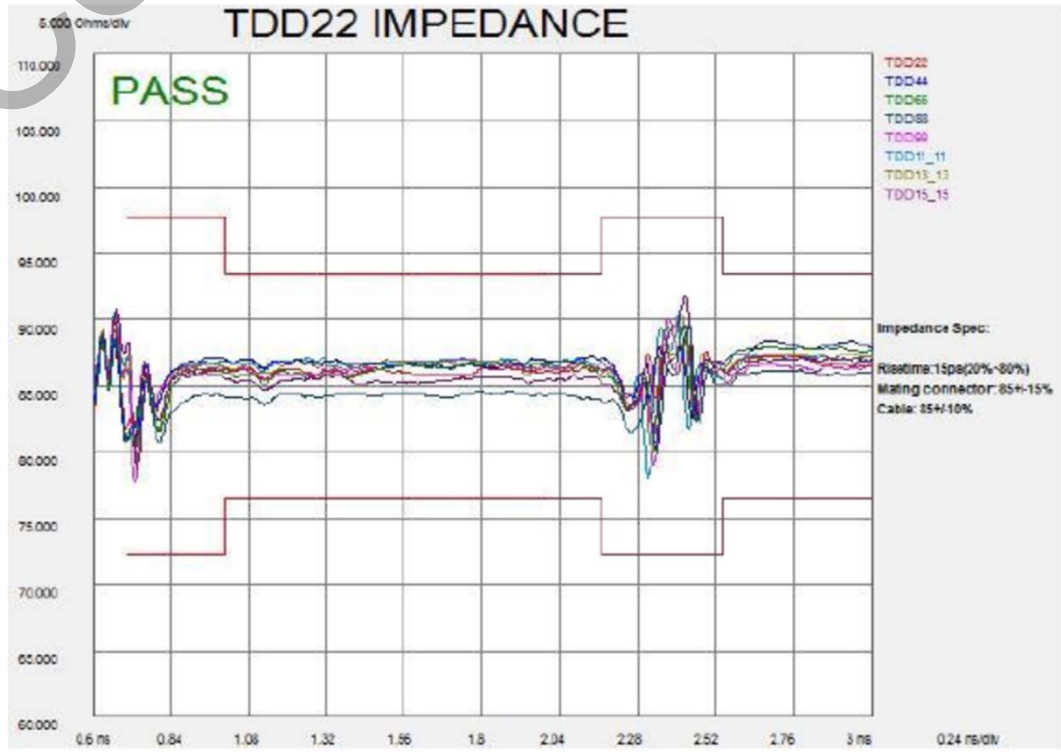
Benefits of Mechanical

- **Accurate orientation** — Primary and secondary guide features
- **Reliable connection** — Effective contact length up to 1.7mm
- **High density** — Two layers PCB, high density with small form factor

Blind Mate

SI measured data based on proposed PCIe Gen5 standard, 30AWG 480mm MCIO to blind mate to MCIO





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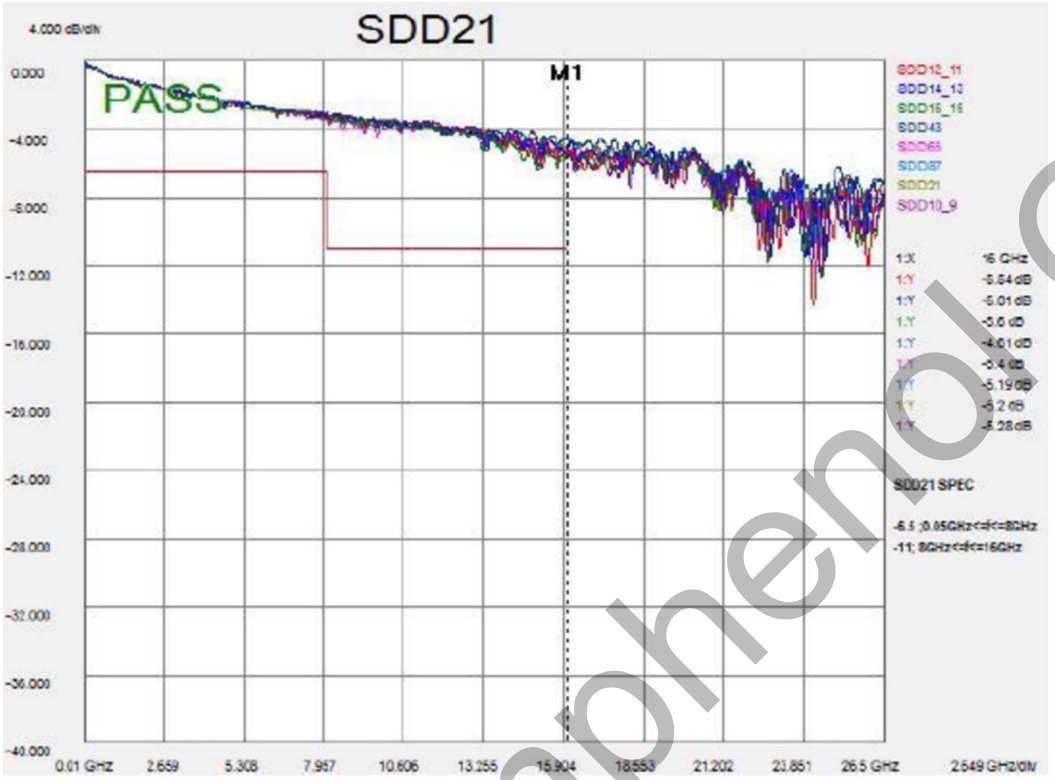
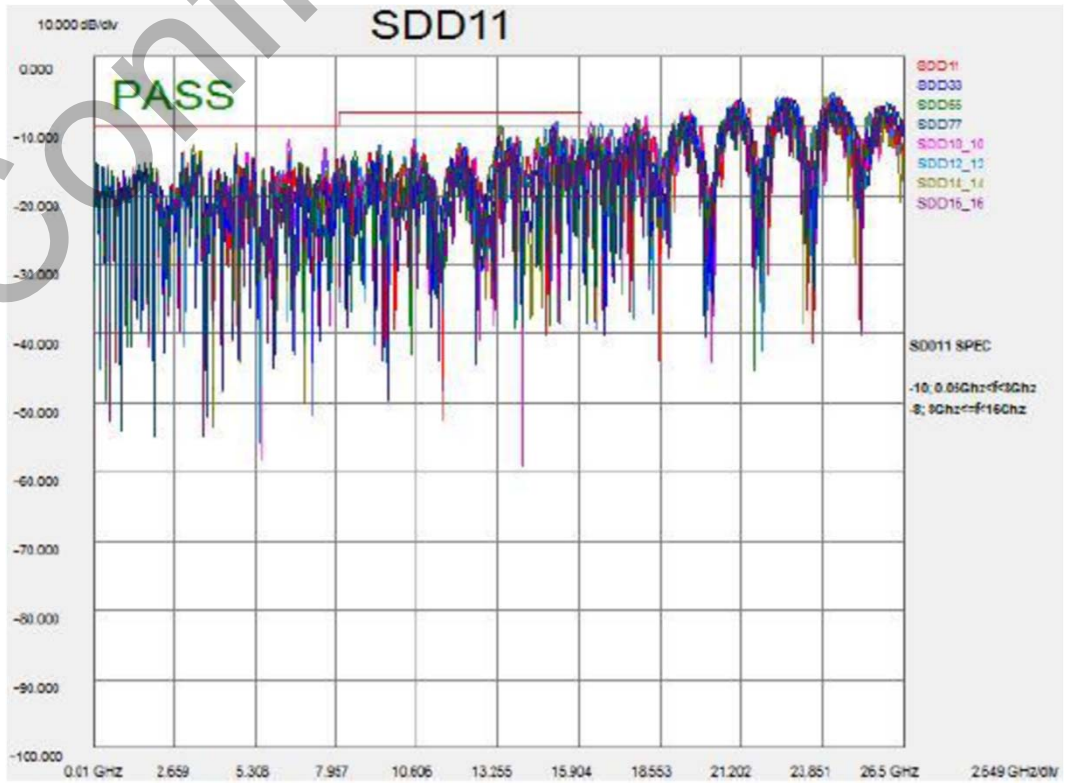
Blind Mate

SI measured data based on proposed PCIe Gen5 standard, 30AWG 480mm MCIO to blind mate to MCIO





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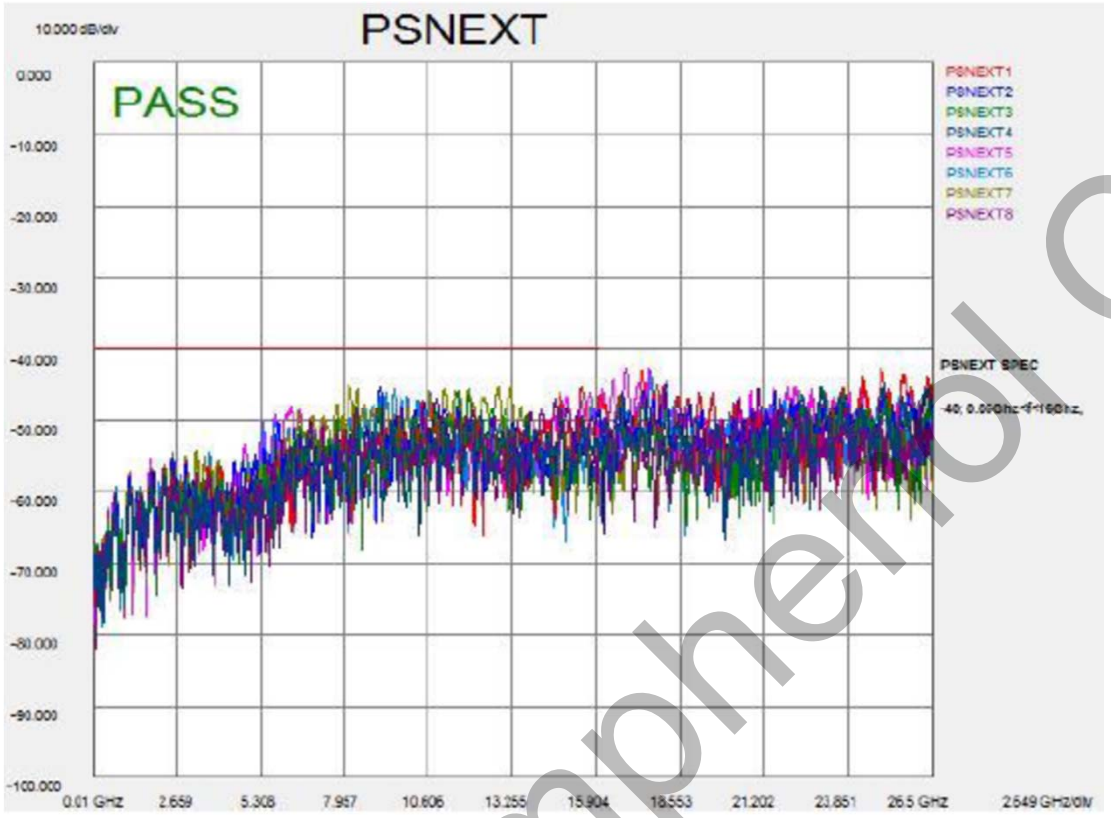
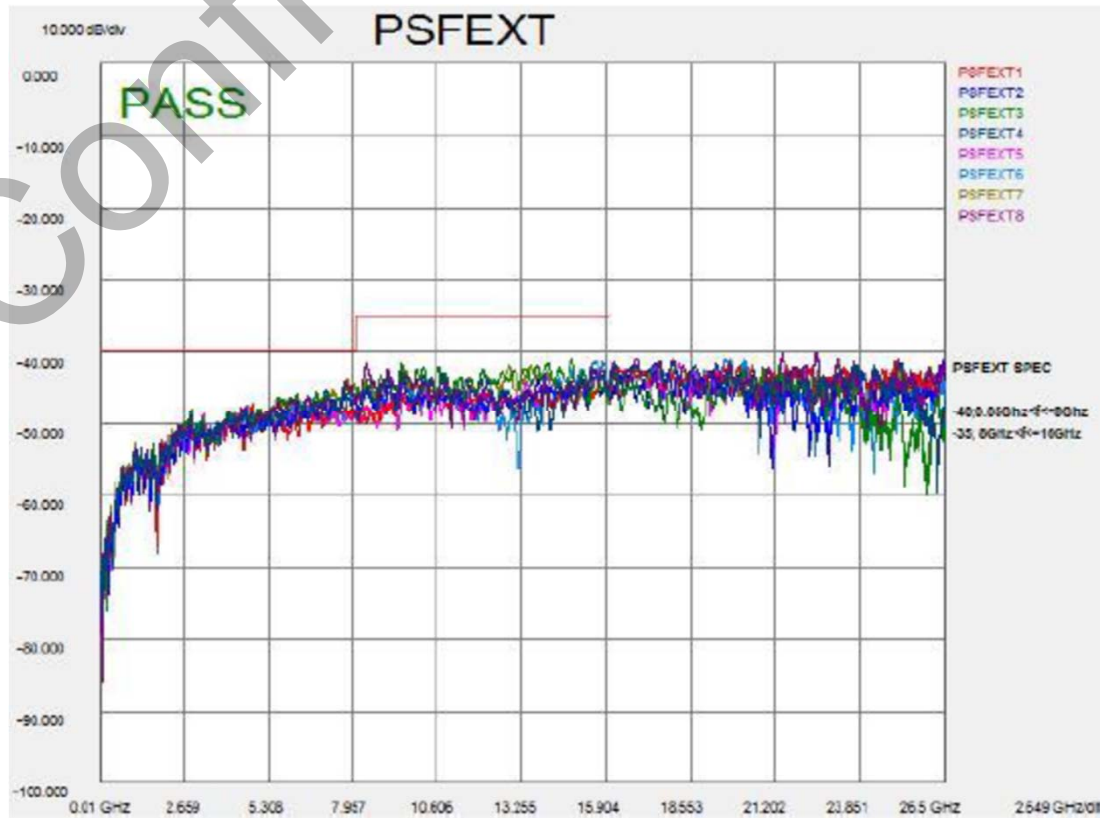
Blind Mate

SI measured data based on proposed PCIe Gen5 standard, 30AWG 480mm MCIO to blind mate to MCIO





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Blind Mate

Benefits of SI

- **IL** — Typical IL -6.4dB @ 16GHz (480mm)
- **Crosstalk** — Typical NEXT is -45dB, FEXT is -41dB @ 16GHz
- **Impedance** — Supports 85ohm±10%(RT=15ps)

Blind Mate

Highlight

IL

- Supports proposed PCIe Gen5 standard
- Scalable to support PCIe Gen6 standard

Mechanical

- Primary and secondary guide and allowable tolerance 1.5mm

Application

- Multiple mother boards, chip to chip

Extremeport-MCIO

MCIO

MCIO is an industrial standard interface of SFF-TA-1016 and PCI-SIG Gen5. SI performance can support PCIe Gen5 and PCIe Gen6. The mating height of 11.95mm is an option for special applications. The impedance supports both 85-ohm and 95-ohm solutions.

SI

- Supports proposed PCIe Gen5 standard
- Scalable to support PCIe Gen6 and SFF-TA-1002 112G PAM4

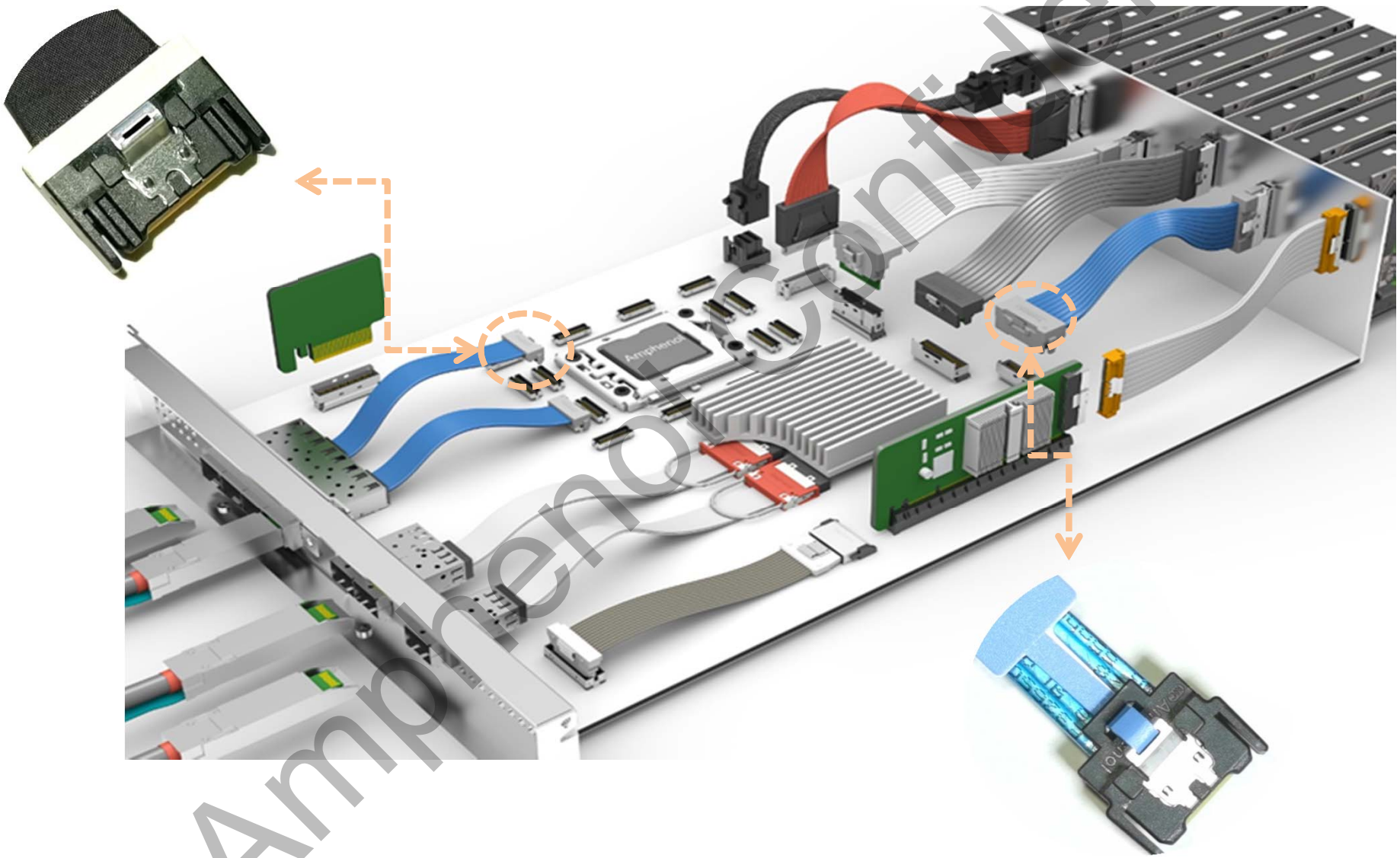
Mechanical

- Typical mating height 14.95mm and optional for special application11.95mm

Application

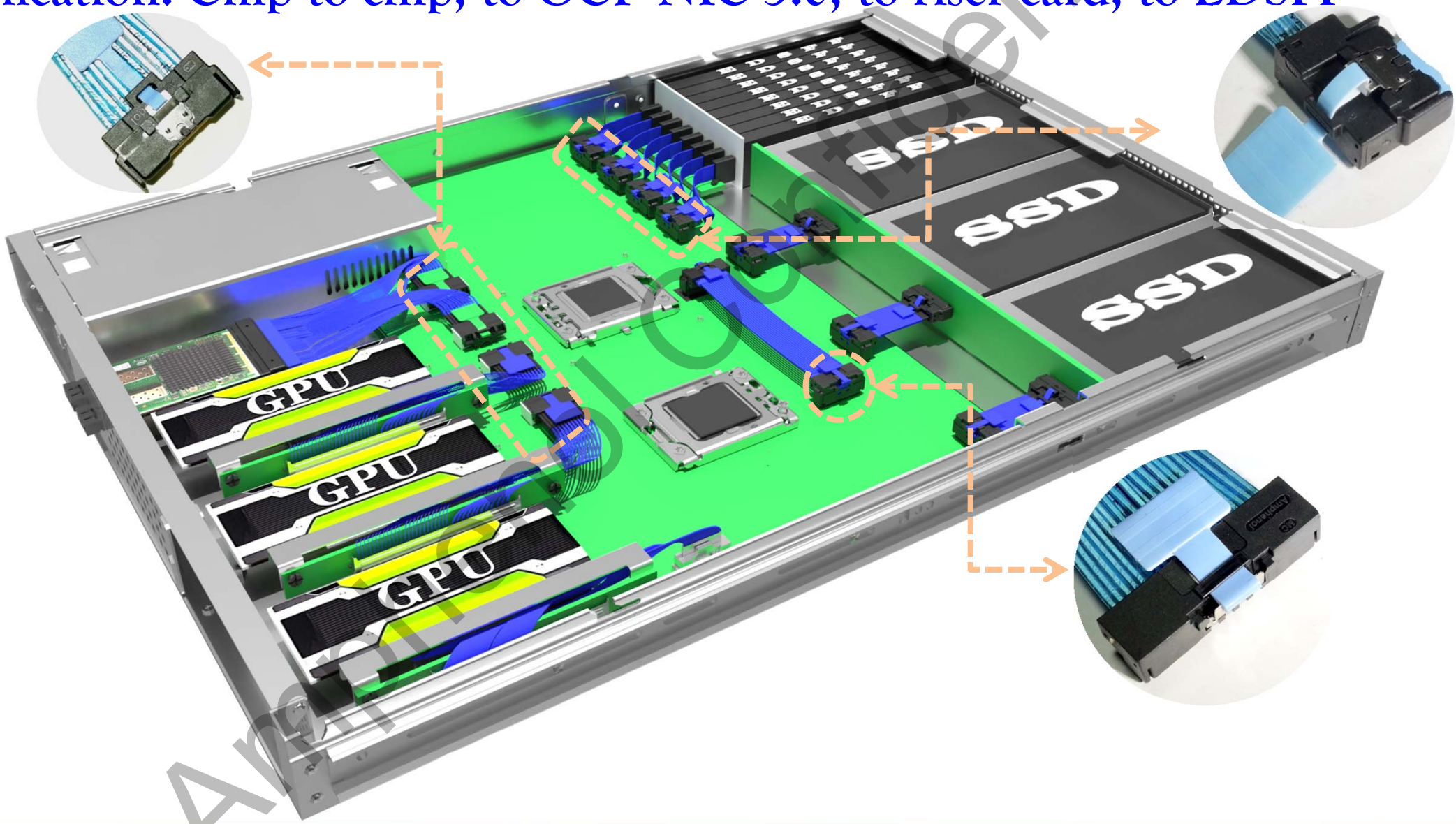
- Supports chip to backplane, to chip, to riser, to IO

Application: chip to IO, chip to backplane



MCIO

Application: Chip to chip, to OCP NIC 3.0, to riser card, to EDSFF



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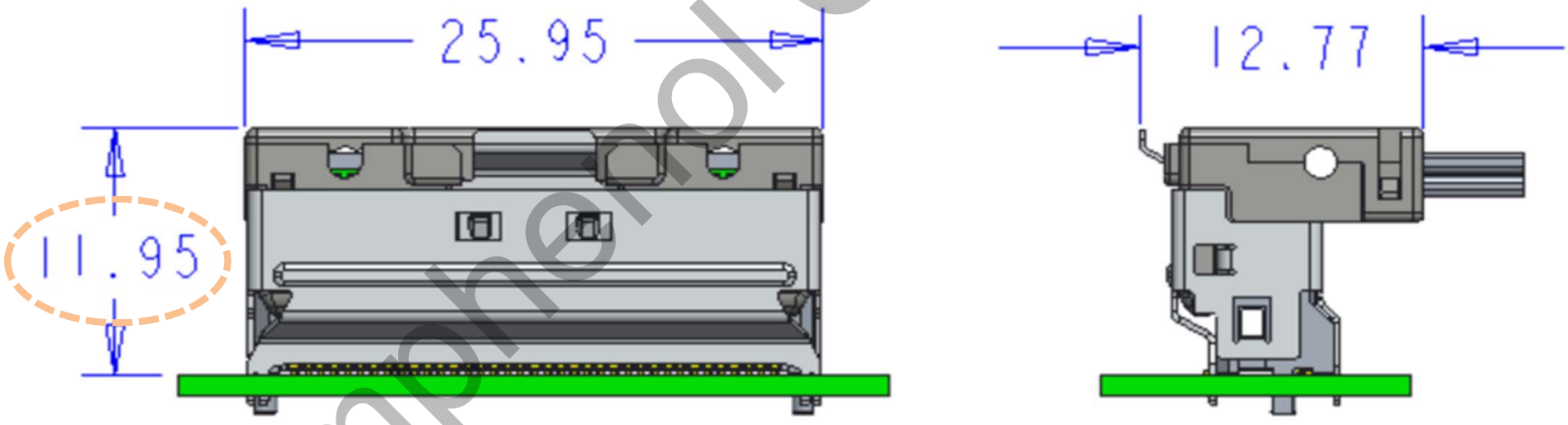
Benefits of application

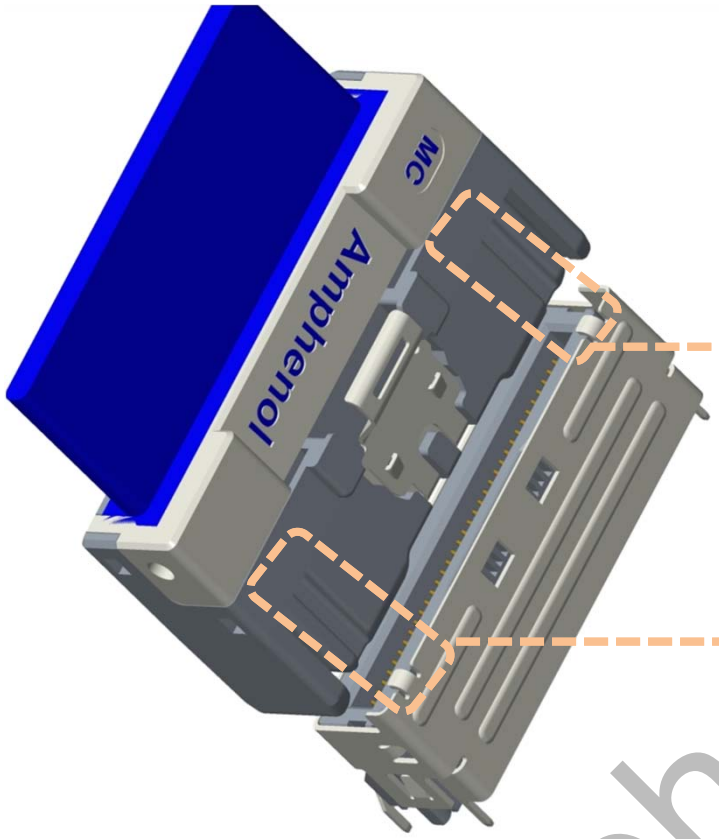
- **Leading position**: SFF-TA-1016 and PCI SIG for PCIe Gen5 (85ohm solution)
- **Excellent SI**: Supports proposed PCIe Gen5 and PCIe Gen6 standard
- **Multiple impedance**: Supports 85ohm and 95ohm application

Mechanical: Mating height 11.95mm is customized for special application and 74pin sample is available.

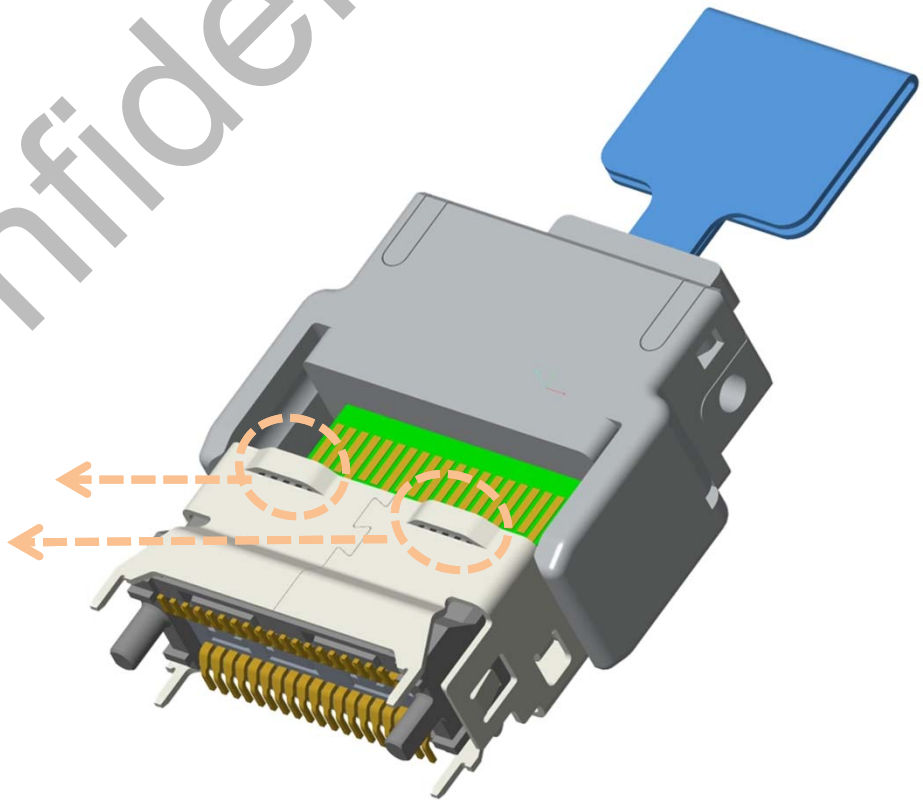
Mating height 11.95mm
(R/A plug with vertical board connector)



Mechanical: Anti-reverse feature



Anti-reverse feature is available



MCIO 95ohm feature

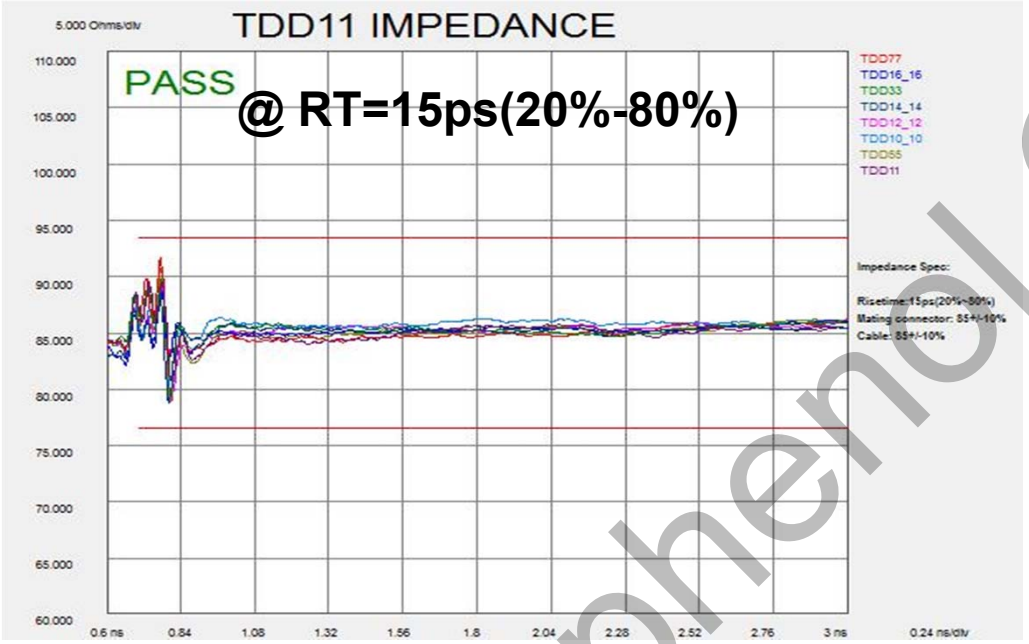
MCIO 85ohm feature

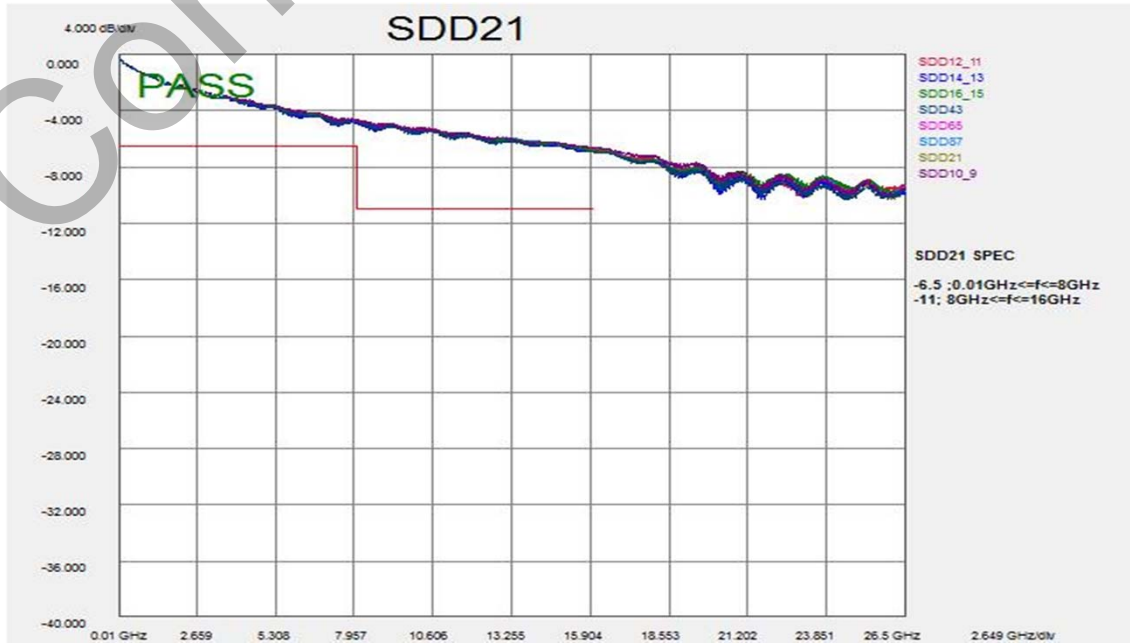
Benefits of Mechanical

Robust	Anti-skew and anti-reverse feature
Low mating height	Typical mating height is 14.95mm and11.95mm mating height is an option for special application
Connector type	38p, 50p, 74p, 84p, 100p, 124p, 148p with RA, STR and SE

MCIO_PCIe Gen5

Measured SI data based on proposed PCIe Gen5 standard, 1000mm 30AWG cable, STR plug with V/T receptacle





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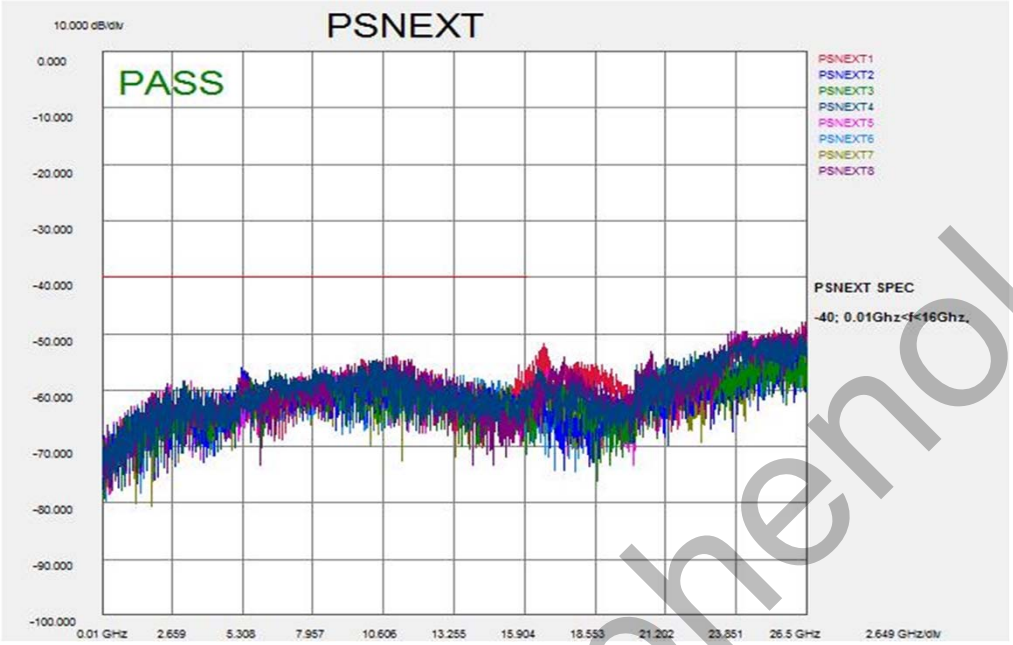
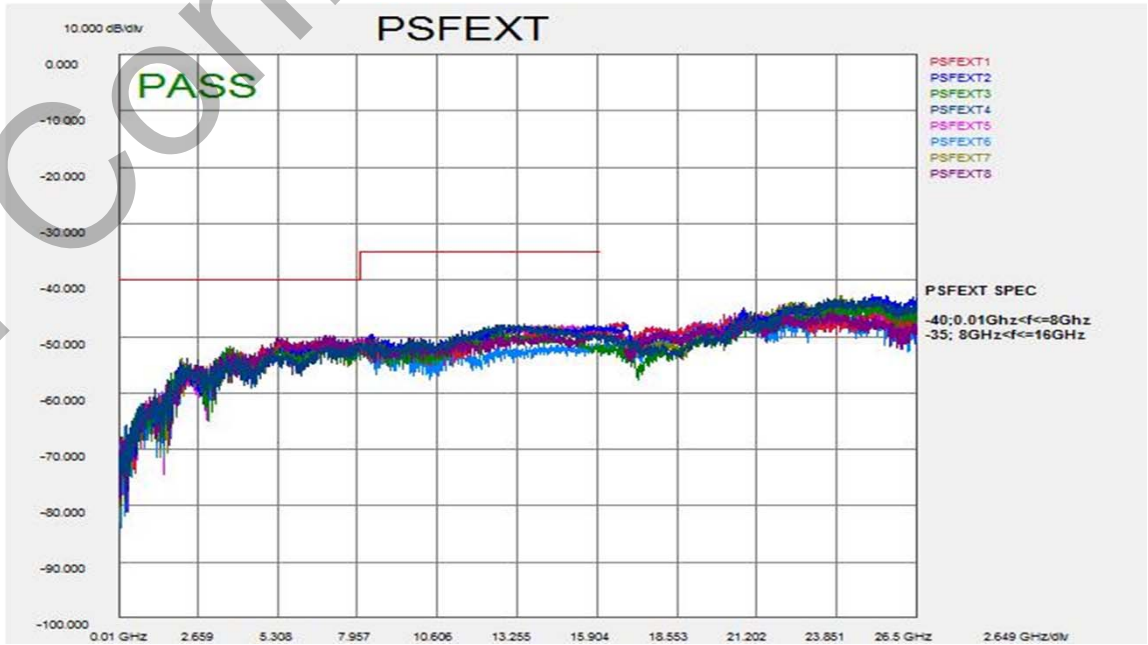
MCIO_PCIe Gen5

Measured SI data based on proposed PCIe Gen5 standard, 1000mm 30AWG cable, STR plug with V/T receptacle





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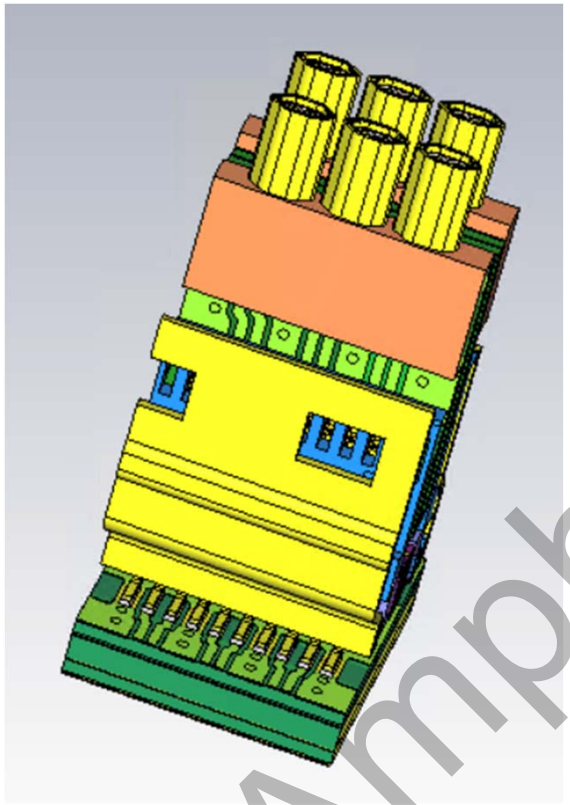
Benefits of SI

- **IL** — Typical IL is 6.89dB @ 16GHz (1000mm)
- **Crosstalk** — Typical NEXT is -50dB, FEXT is -45dB @ 16GHz
- **Impedance** — Supports 85ohm±10% and 95ohm±10%(RT=15ps)

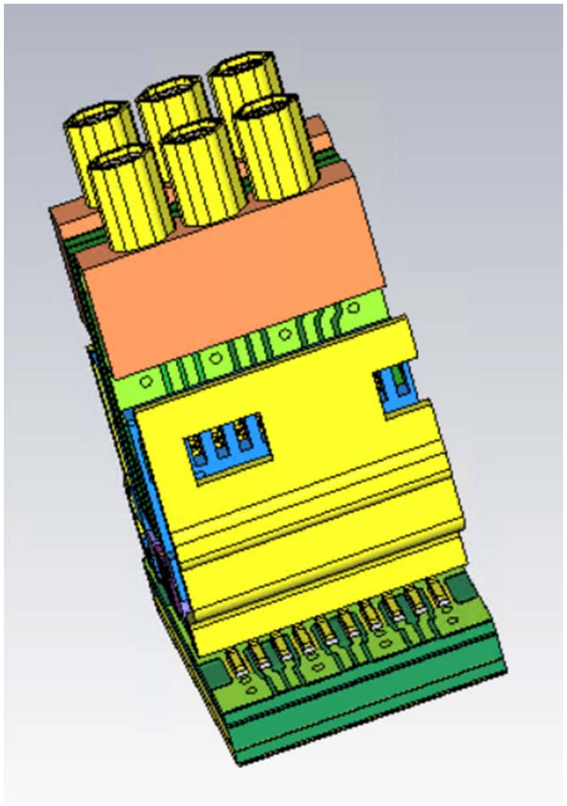
MCIO_PCIe Gen6

SI simulation data is based on improved MCIO STR plug with V/T receptacle. 1000mm 29AWG raw cable is used to cascaded into cable assembly.

Proposed PCIe Gen6 cable spec (1000mm) is used.



1000mm 29AWG Raw Wire



MCIO_PCIe Gen6

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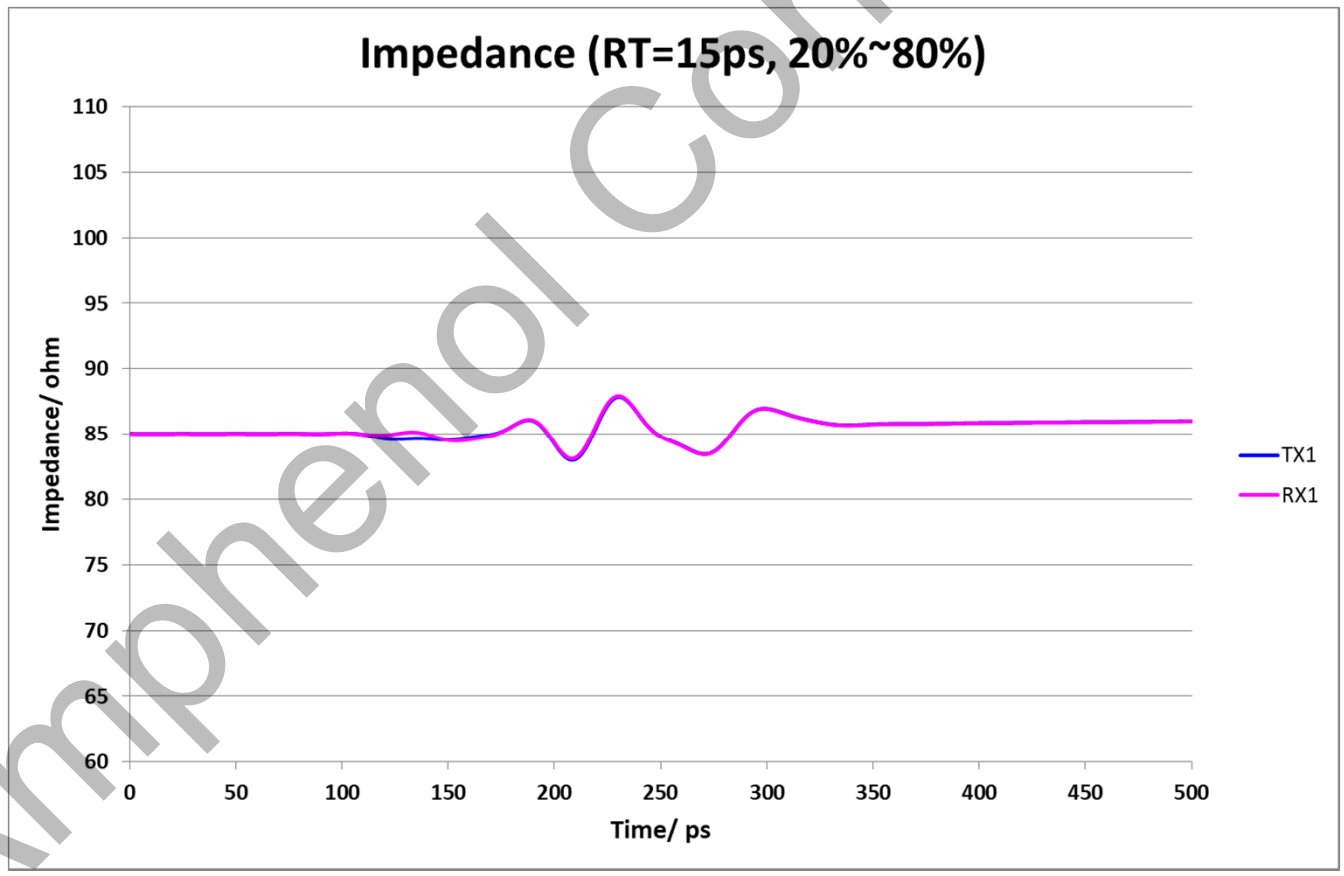
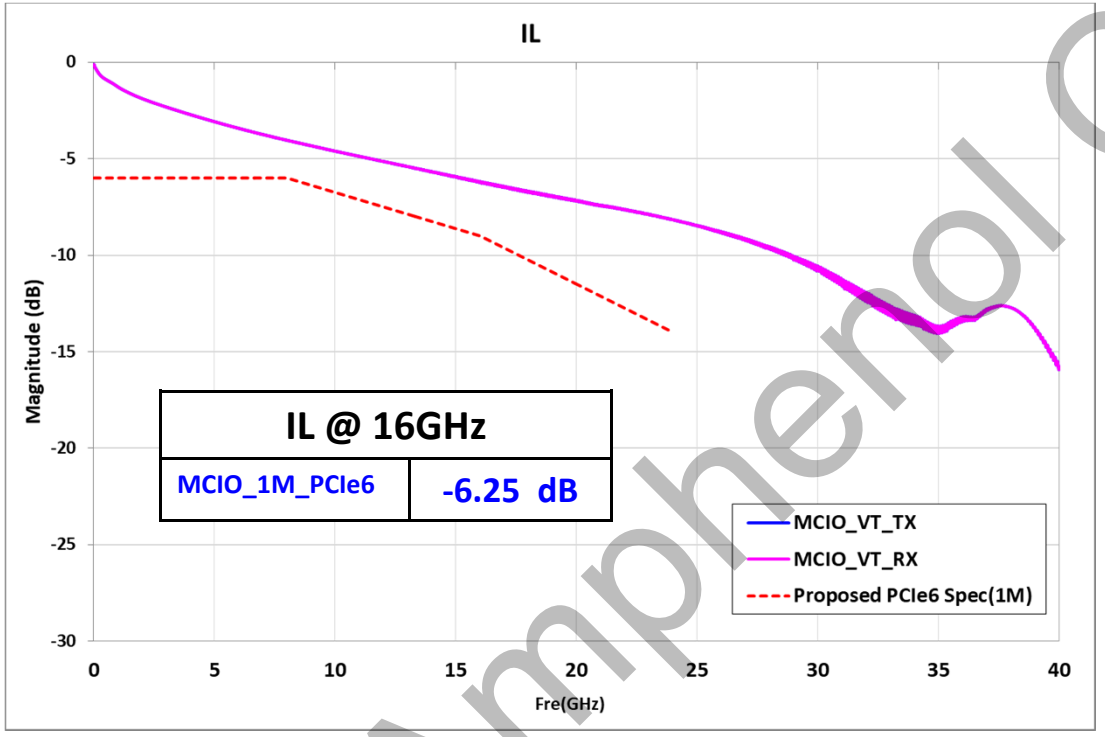


Amphenol

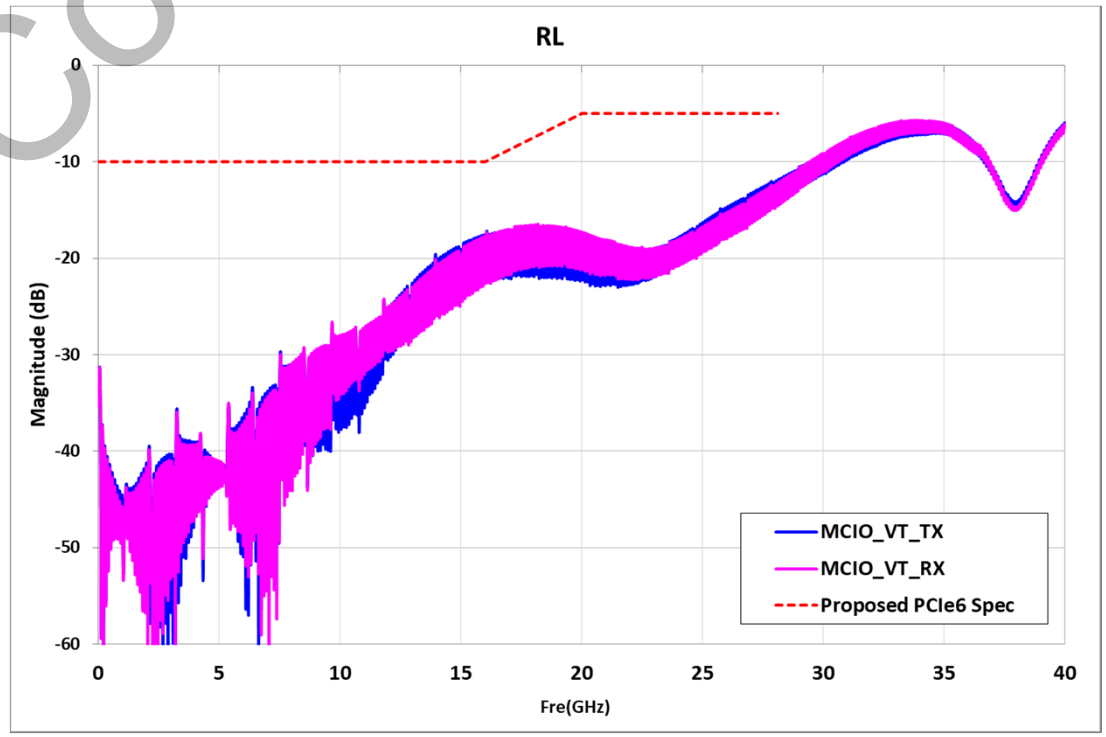
MCIO_PCIe Gen6

SI simulation data is based on improved MCIO STR plug with V/T receptacle. 1000mm 29AWG raw cable is used to cascaded into cable assembly.

Proposed PCIe Gen6 cable spec (1000mm) is used.



IL @ 16GHz	
MCIO_1M_PCIe6	-6.25 dB



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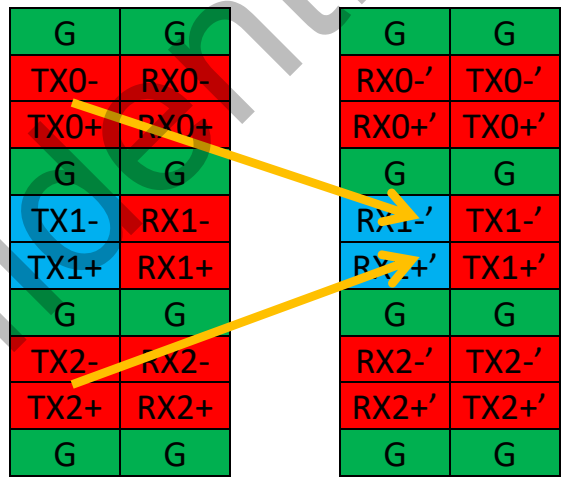
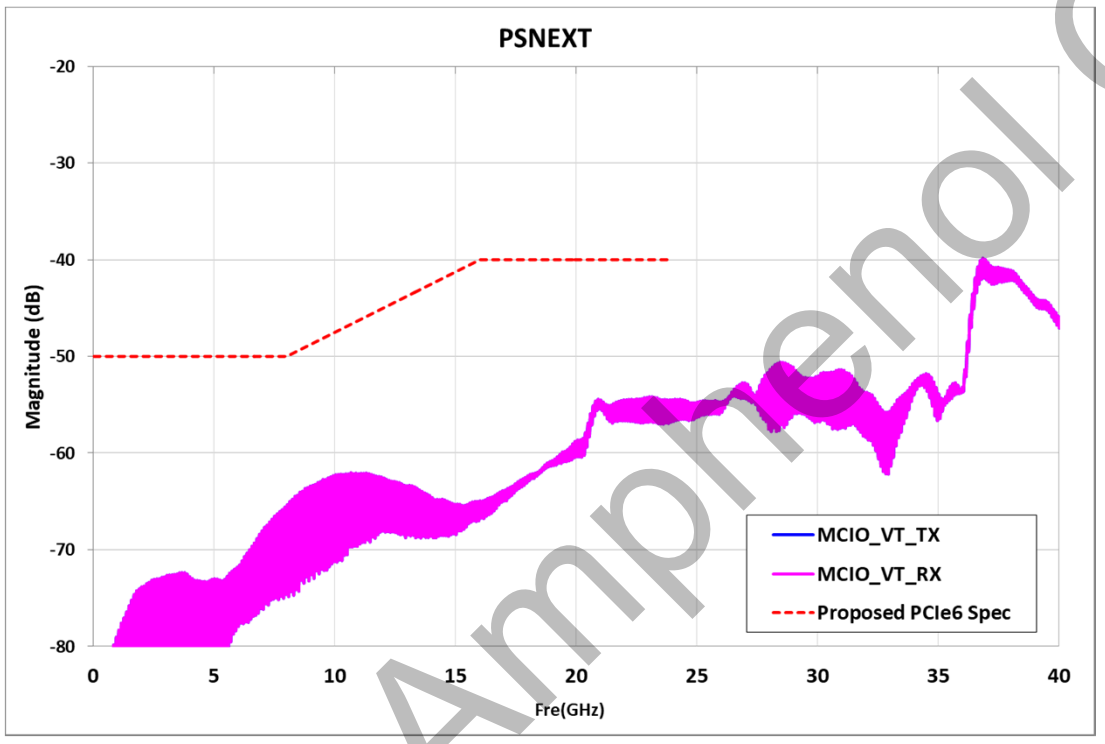
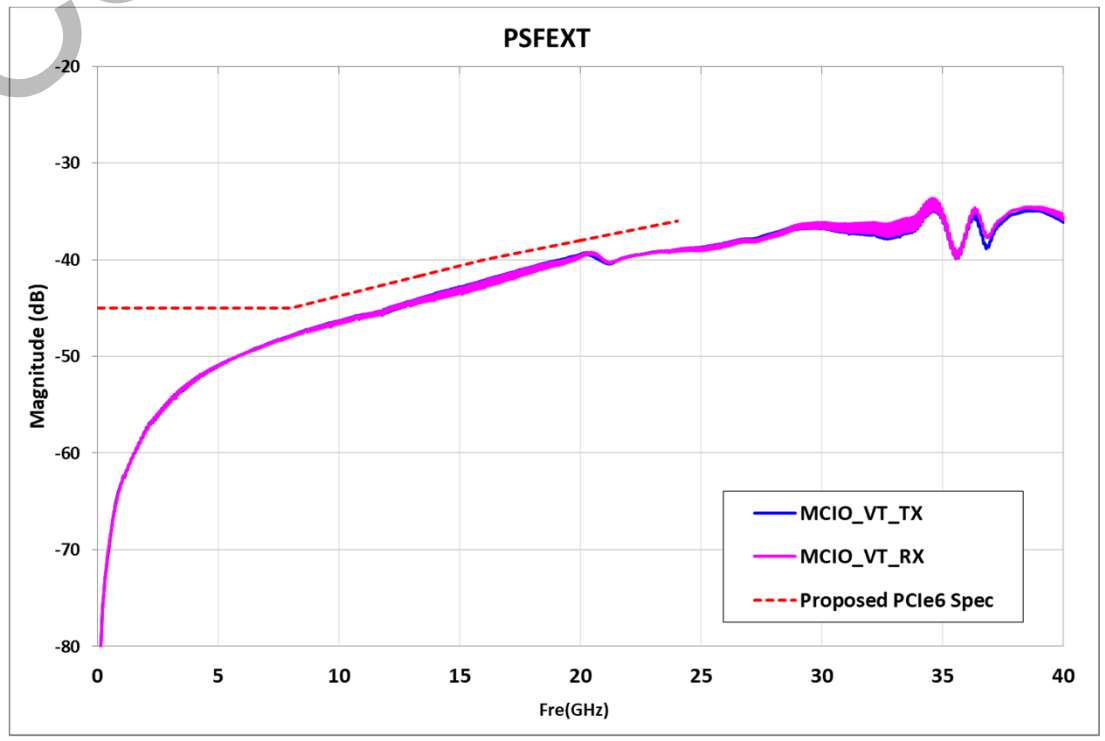
MCIO_PCIe Gen6

G	G
TX0-	RX0-
TX0+	RX0+
G	G
TX1-	RX1-
TX1+	RX1+
G	G
TX2-	RX2-
TX2+	RX2+
G	G

G	G
RX0-’	TX0-’
RX0+’	TX0+’
G	G
RX1-’	TX1-’
RX1+’	TX1+’
G	G
RX2-’	TX2-’
RX2+’	TX2+’
G	G





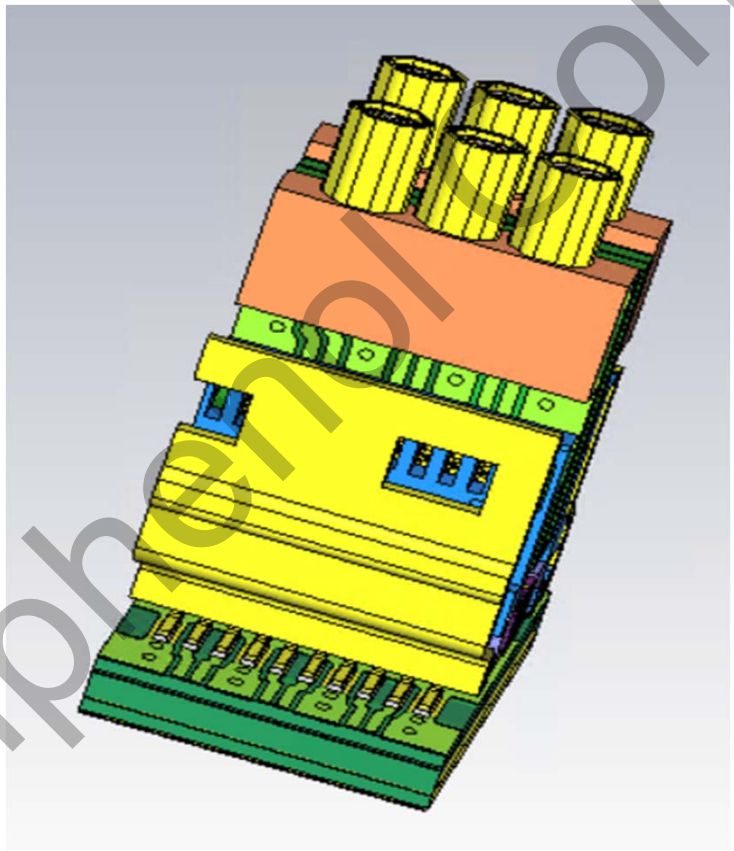


Amphenol

MCIO_112G PAM4

SI simulation data is based on improved MCIO STR plug with V/T receptacle, wire termination considered.

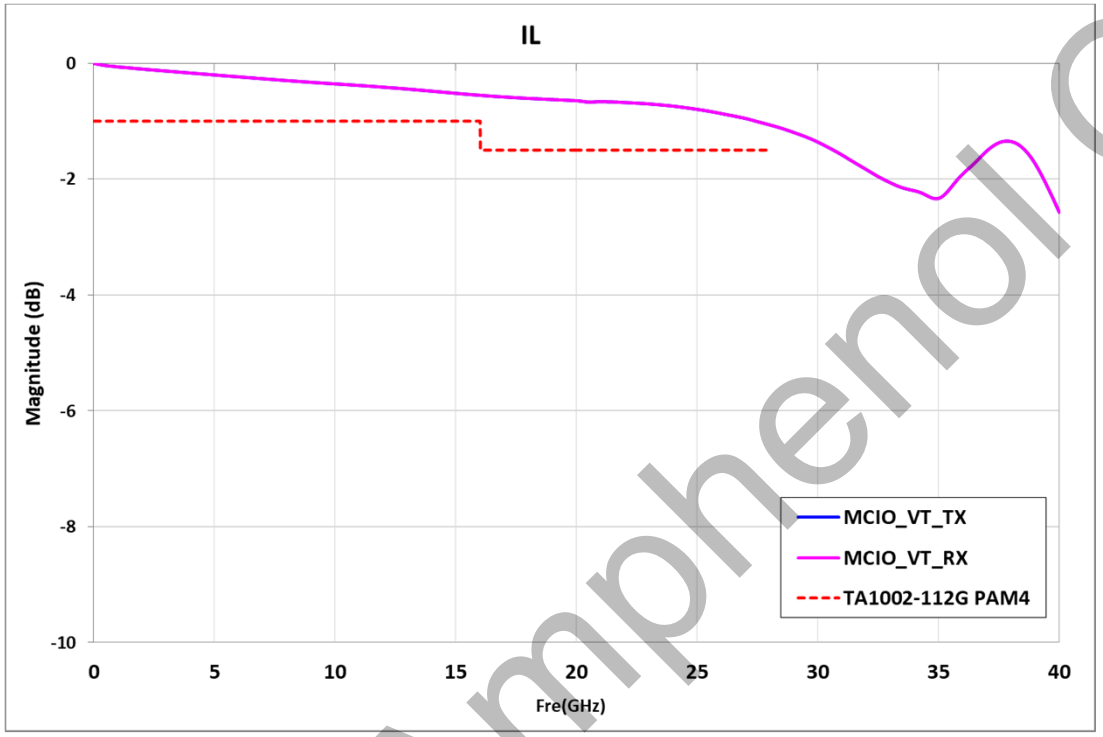
SFF-TA-1002 112G PAM4 spec used is for connector only.
(*Our model with termination considered still pass with good margin.)

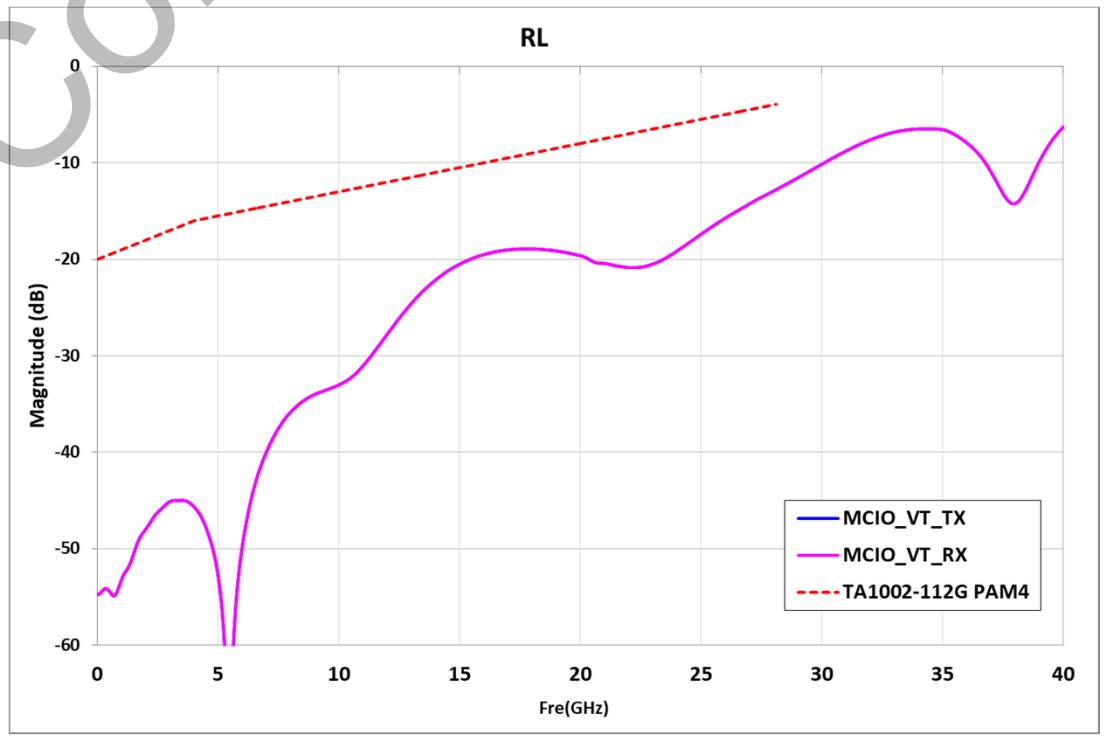


MCIO_112G PAM4

SI simulation data is based on improved PCIe6 MCIO STR plug with V/T receptacle, wire termination considered.

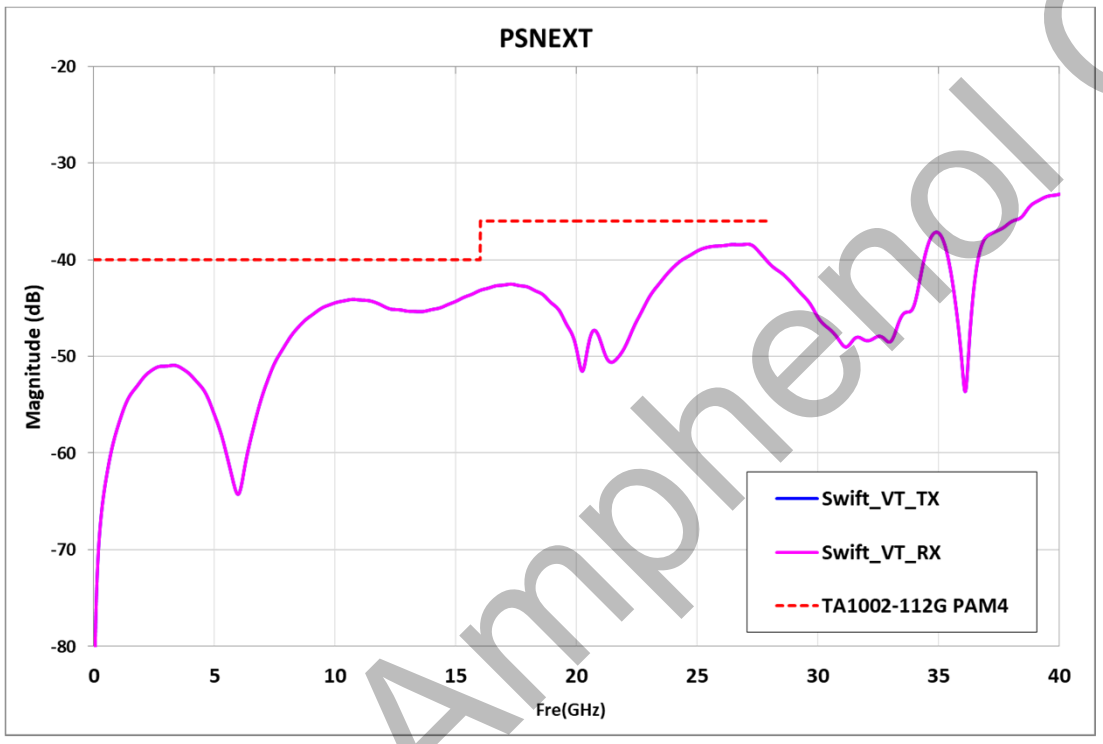
SFF-TA-1002 112G PAM4 spec used is for connector only.
(*Our model with termination considered still pass with good margin.)

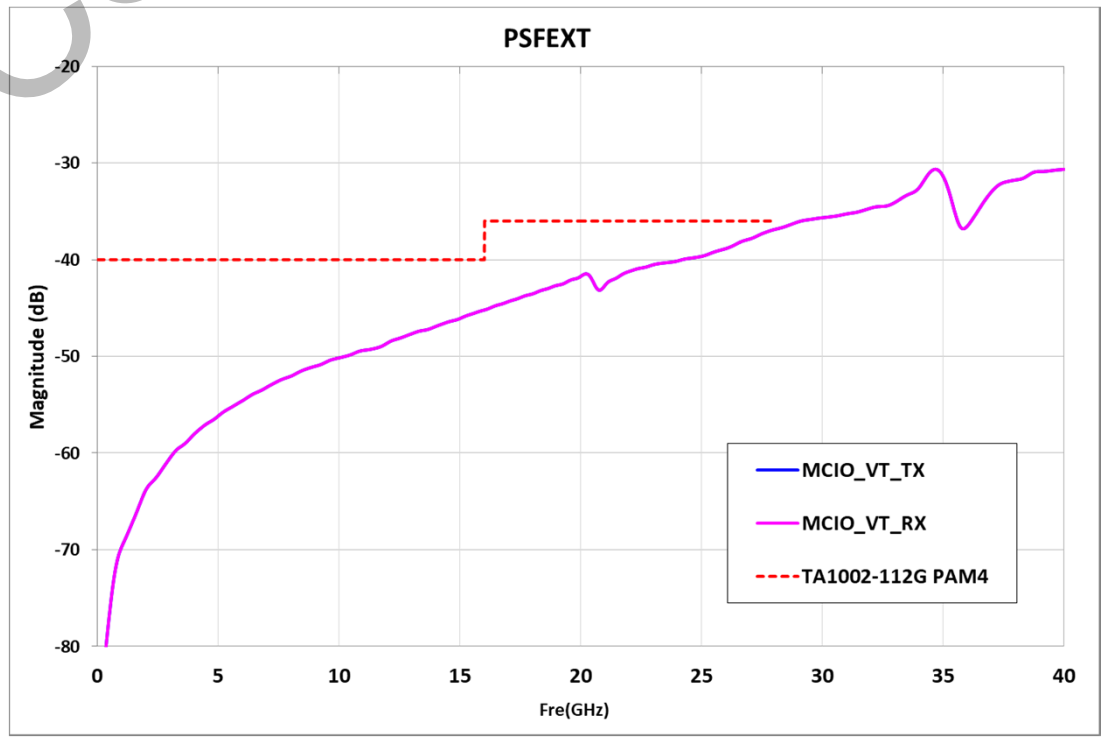




Amphenol

MCIO_112G PAM4





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Configuration matrix: 85ohm version

Channels		4X+S(6X)	4X+S+P	8X	8X+S(12X)	8X+S+P	16X	16X+S(20X)	16X+S+P	24X
Pin no.		38pin	56pin	50pin	74pin	84pin	100pin	124pin	140pin	148pin
Status	85 ohm	Available	TBD	Available	Available	STR / RA Available	TBD	Available	TBD	Available

*MCIO 50pin, 56pin, 84pin(1.1A/pin), 100pin and 140pin **are customized connectors, not in SFF-TA-1016 Rev 1.0.**

Configuration matrix: 95ohm version

Channels		4X+S(6X)	8X	8X+S(12X)	16X	16X+S(20X)
Pin no.		38pin	50pin	74pin	100pin	124pin
Status	95ohm	STR / RA Available	Available	STR / RA Available	STR / RA Available	RA Available

MCIO

Highlight

IL

- Typical IL is -6.89dB @ 16GHz (1000mm)

Mechanical

- Robuster, anti-skew and anti-reverse features

Application

- Multiple connector types, different PIN count

SFF-TA-1002

SFF-TA-1002

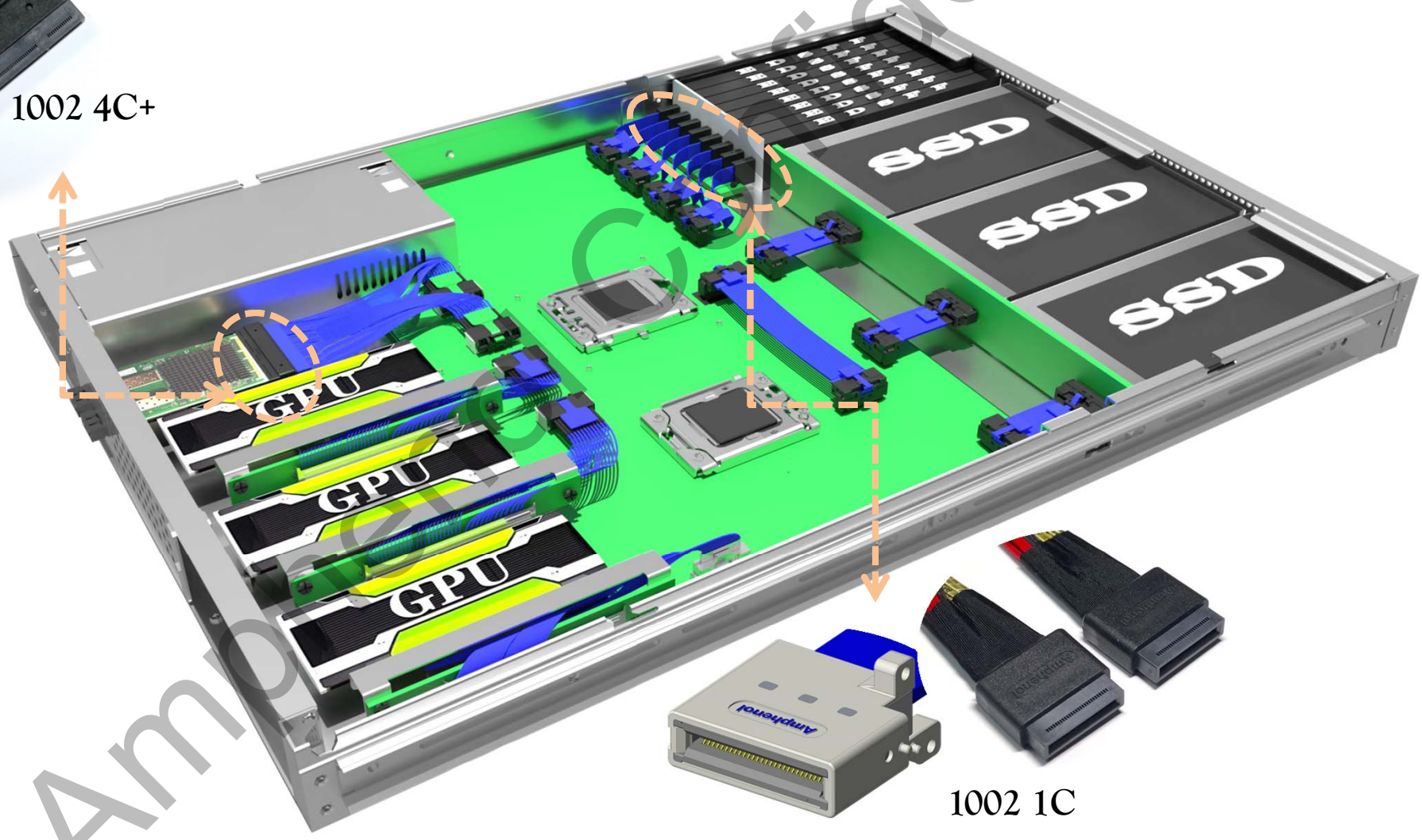
SFF-TA-1002 SI performance meets PCIe Gen5 with lead frame design feature. The interface was adopted by next generation EDSFF and OCP NIC3.0, the full series configuration (1C,2C,4C,4C+) can meet the customer's different applications.

IL	• Supports proposed PCIe Gen5 standard • Scalable to support 112G PAM4
Mechanical	• Die cast shell with orthogonal design feature
Application	• OCP NIC3.0, EDSFF, PECFF

SFF-TA-1002

Applications: Chip to OCP NIC3.0 and chip to EDSFF

1002 4C+



1002 1C

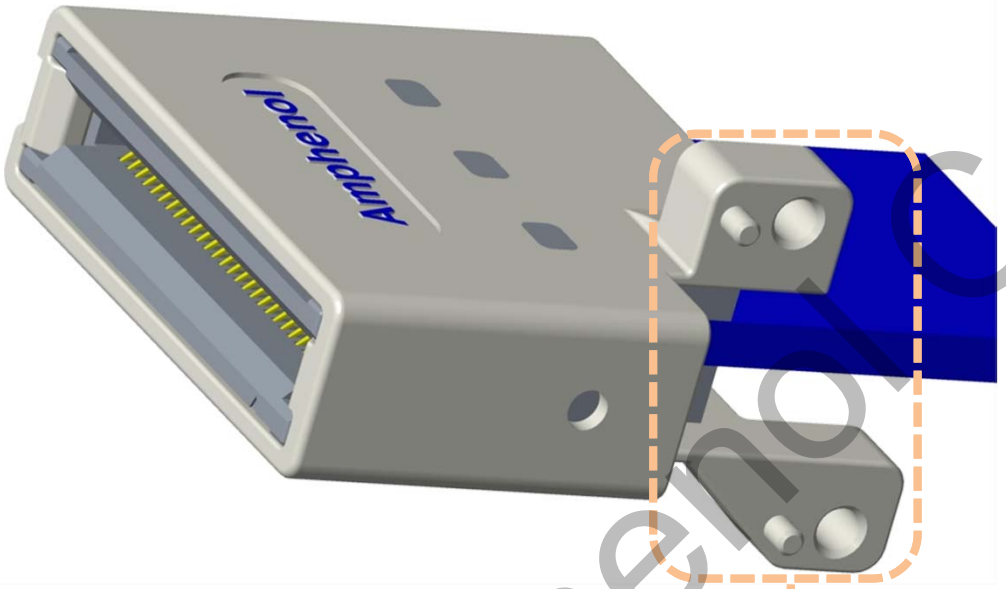
Amphenol

SFF-TA-1002

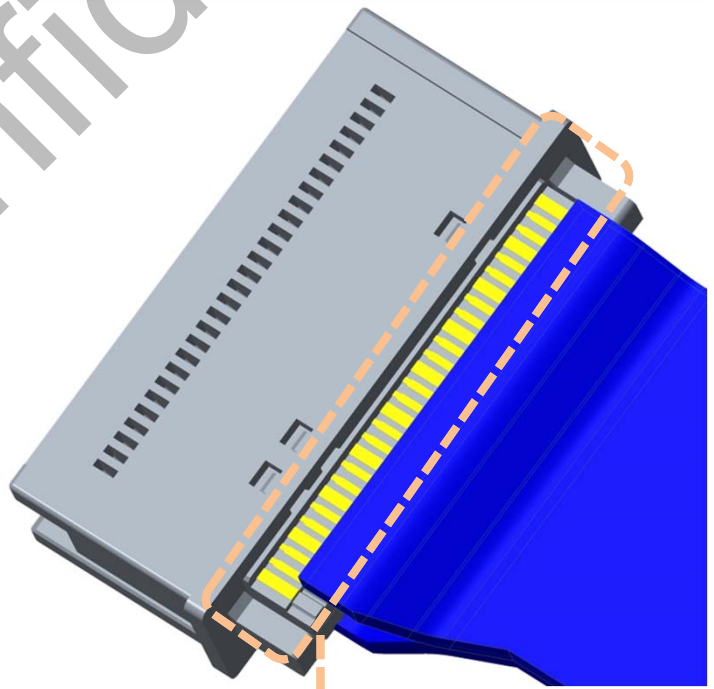
Benefits of application

- **High speed**: Supports proposed PCIe Gen5 standard; Scalable to support 112G PAM4
- **Industrial standard**: Supports Gen-Z, OCP, PECFF, EDSFF interface
- **Connector type**: Supports 1C, 2C, 4C and 4C+

Mechanical: Lead frame and orthogonal feature



Orthogonal design feature to fix the plug for stable connection

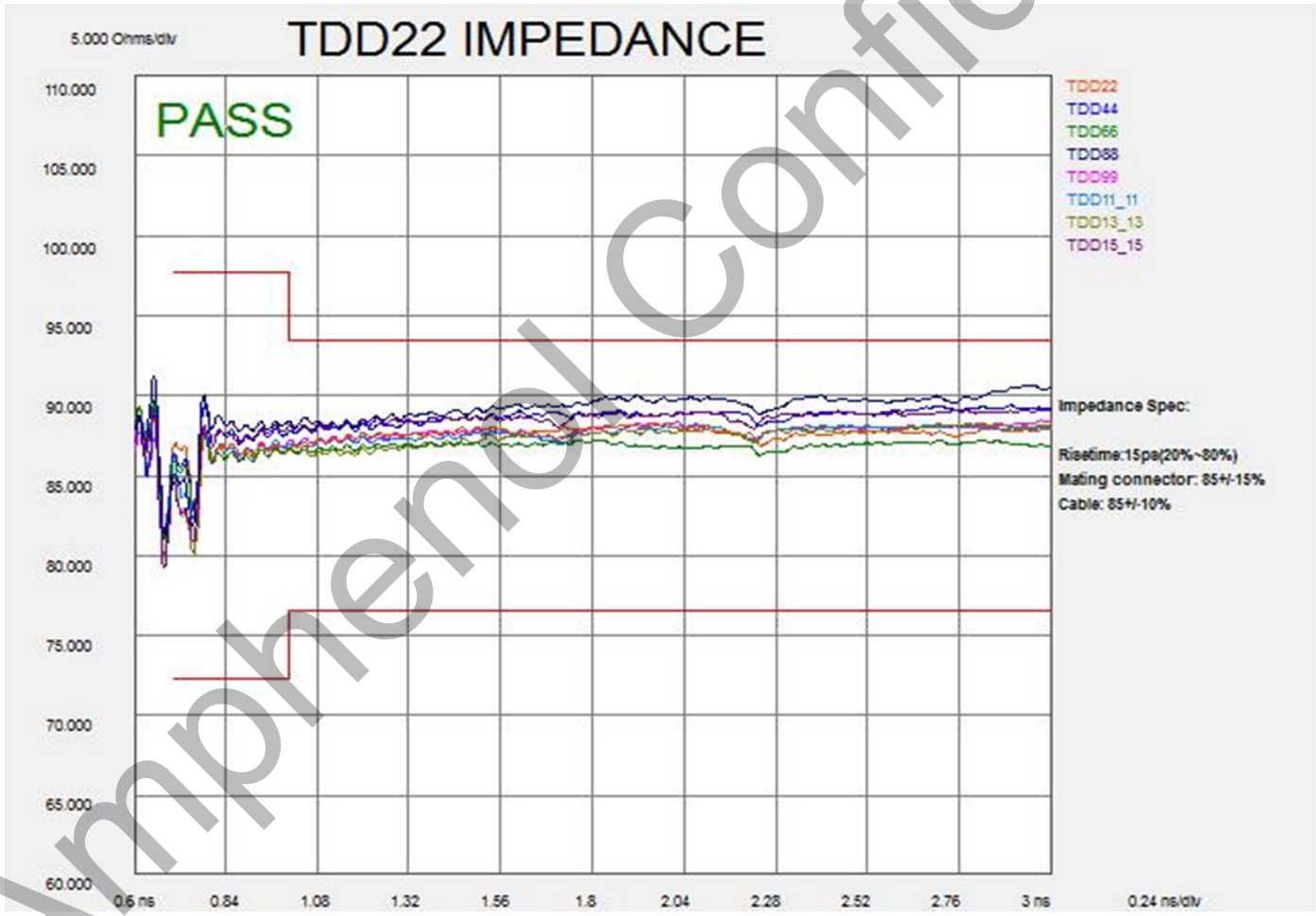


Lead frame design feature

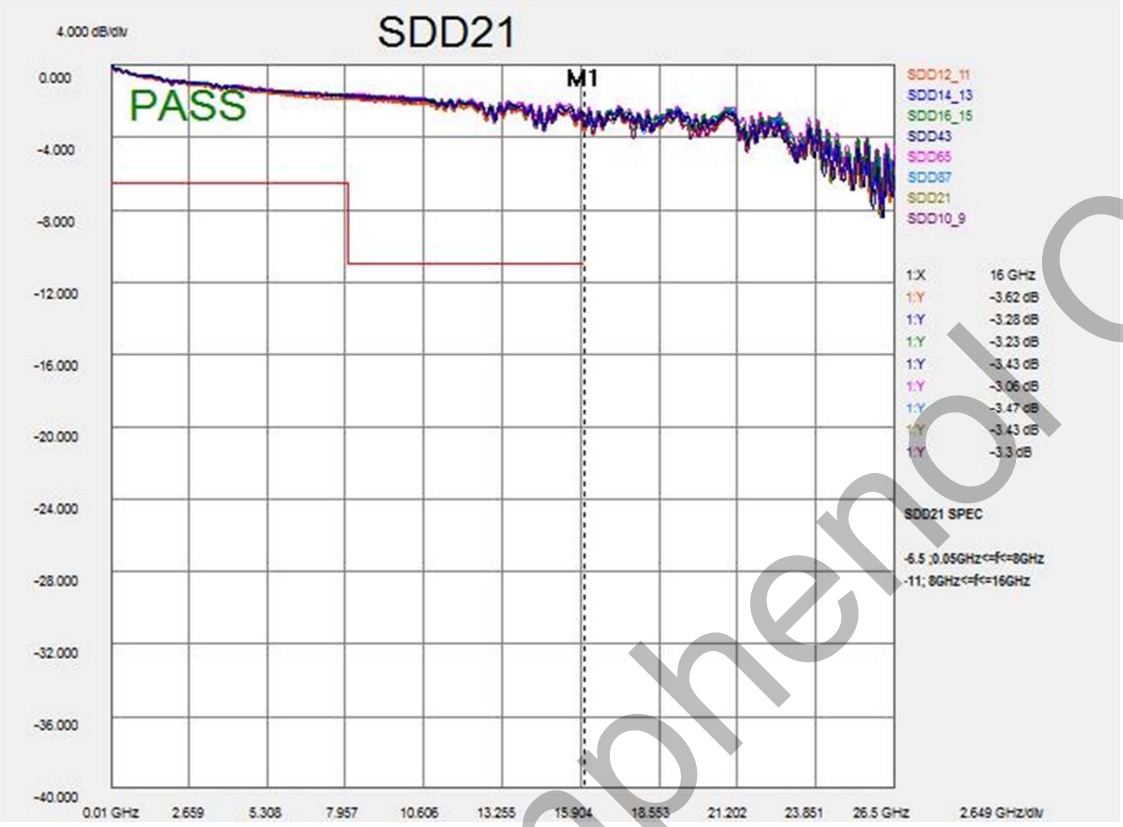
Benefits of mechanical

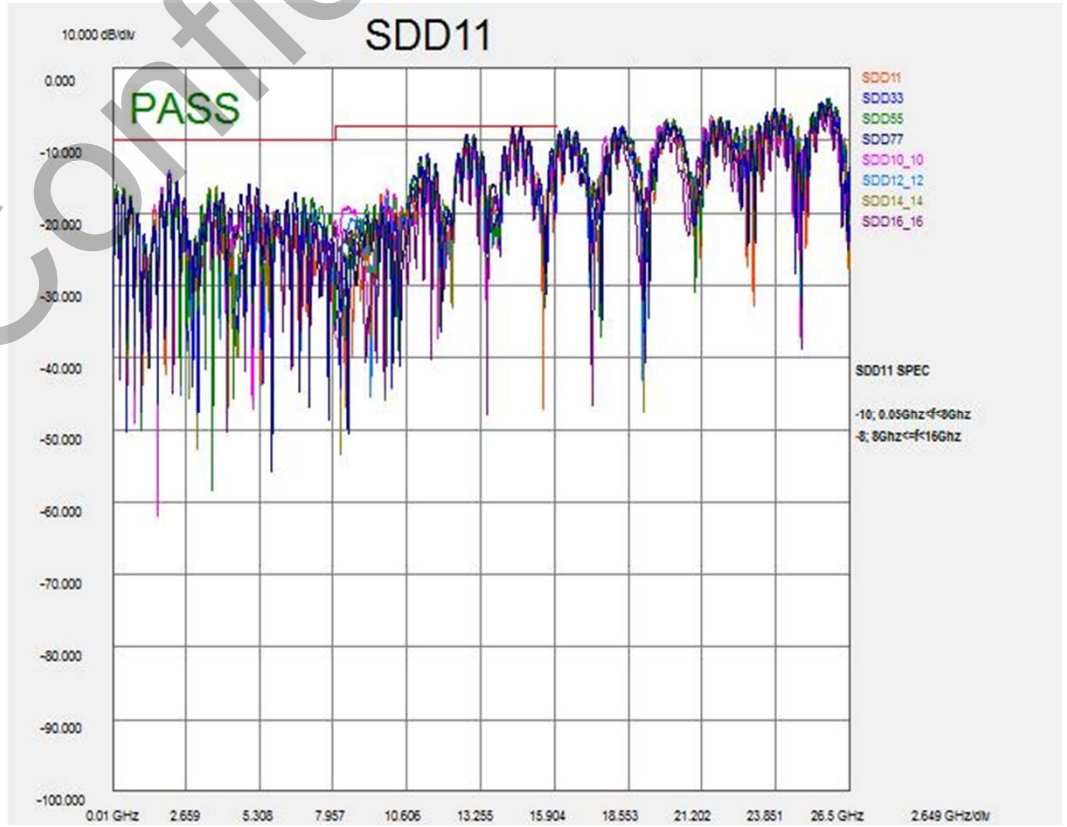
Robust	Die cast shell
Stable connection	0.6mm pitch, orthogonal feature
Optimized process	Lead frame terminal design

SI measured data based on proposed PCIe Gen5 standard, 30AWG 300mm, SFF-TA-1002 to Z-Link



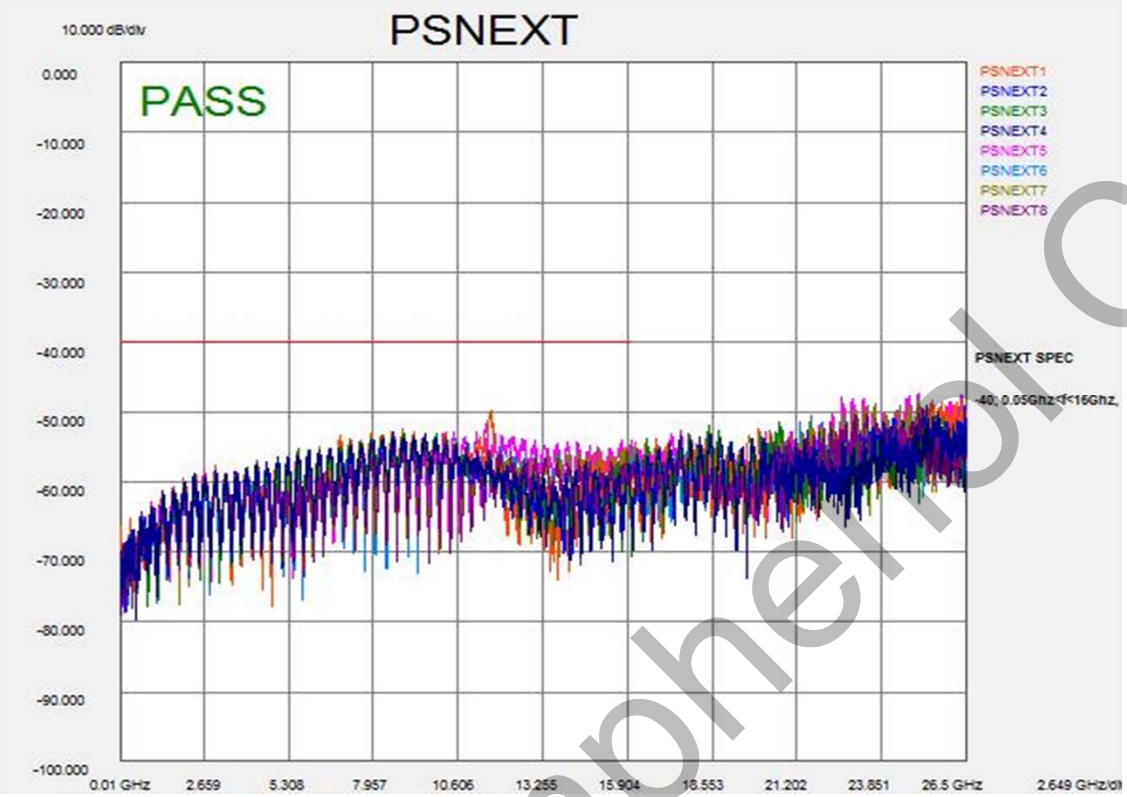
SI measured data based on proposed PCIe Gen5 standard, 30AWG 300mm, SFF-TA-1002 to Z-Link

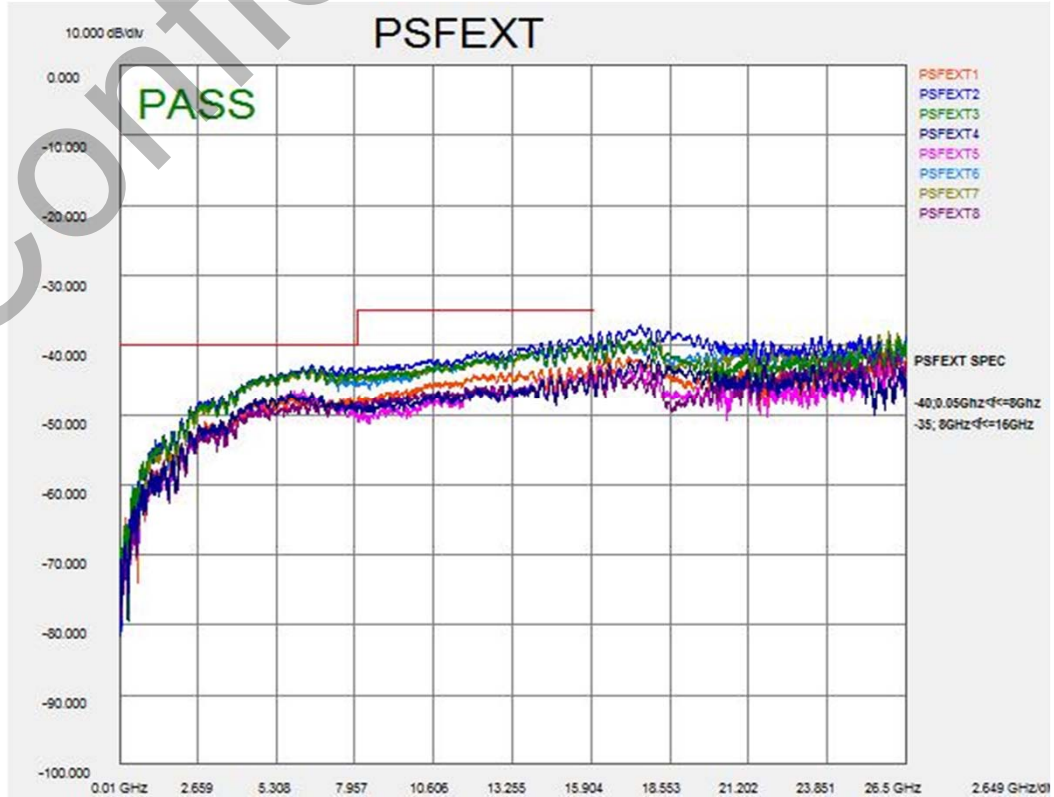




SFF-TA-1002

SI measured data based on proposed PCIe Gen5 standard, 30AWG 300mm, SFF-TA-1002 to Z-Link





Amphenol

Benefits of SI

- **IL** — Typical IL is -3.5dB @ 16GHz (300mm)
- **Crosstalk** — Typical NEXT is -55dB, FEXT is -42dB @ 16GHz
- **Impedance** — Supports 85ohm±10%(RT=15ps)

SFF-TA-1002

Configuration Matrix

Types	1C	2C	4C	4C+
Pin no.	56pin	84pin	140pin	168pin
Channels	4X+S+P	8X+S+P	16X+S+P	16X+S+P
Status	Sample available			

SFF-TA-1002

Highlight

IL

- Supports proposed PCIe Gen5 standard

Mechanical

- Robuster, die cast shell with orthogonal design feature

Application

- Supports OCP NIC3.0, EDSFF, PECFF

Extremeport-Z-Link (SFF-TA-1020)

Z-Link(SFF-TA-1020)

Z-Link is the low-profile version of SFF-TA-1020 and is available in a full series configuration of 0.5C, 1C, 2C, 4C and 4C+. Fully compliant to SFF-TA-1020, OCP, Gen Z alliance and the SI can meet the current PCIe Gen5 standard.

SI

- **Supports proposed PCIe Gen5 standard**

Mechanical

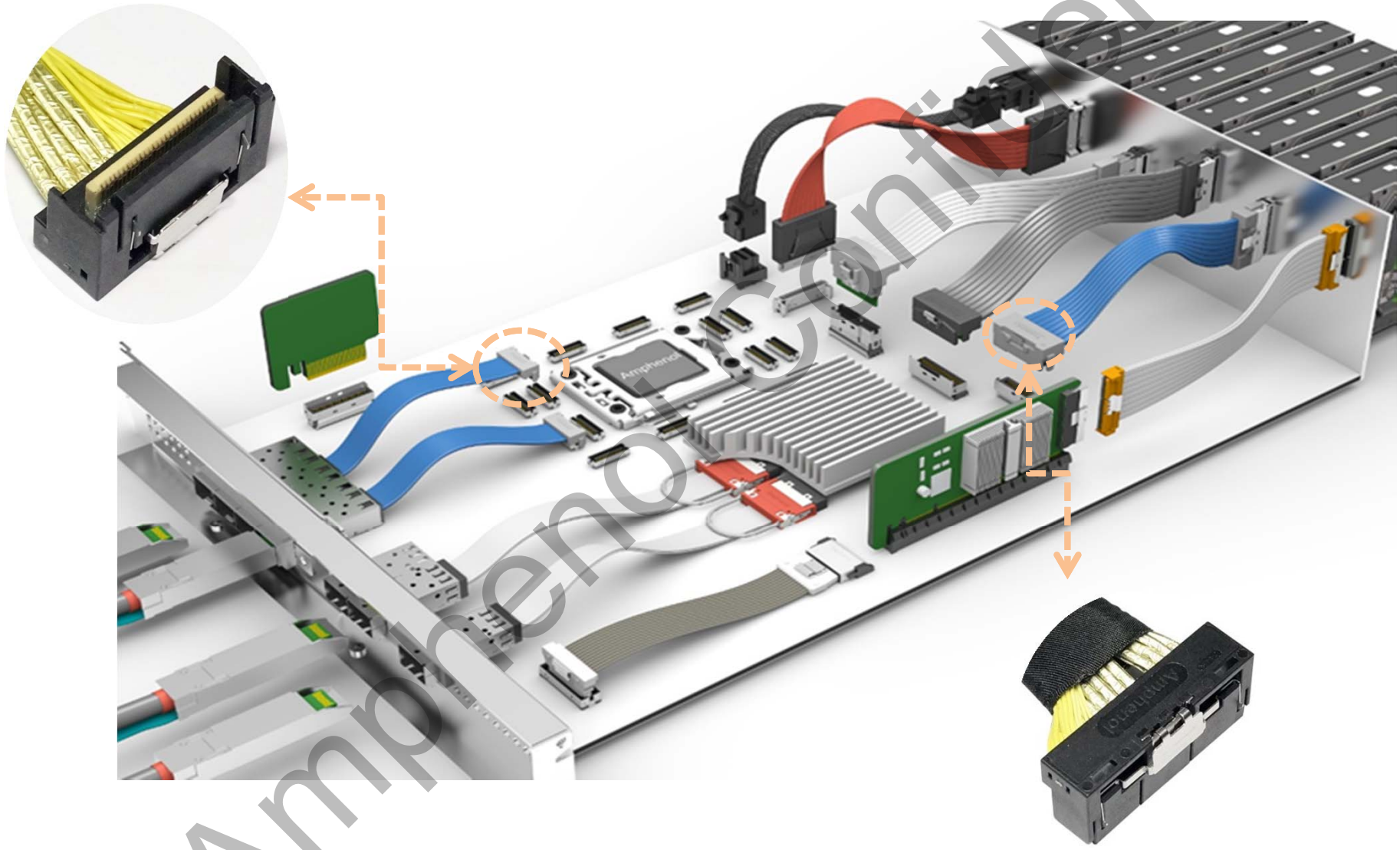
- **Low profile latch with anti-skew feature**

Application

- **Supports chip to backplane, chip to chip, chip to riser, chip to IO**

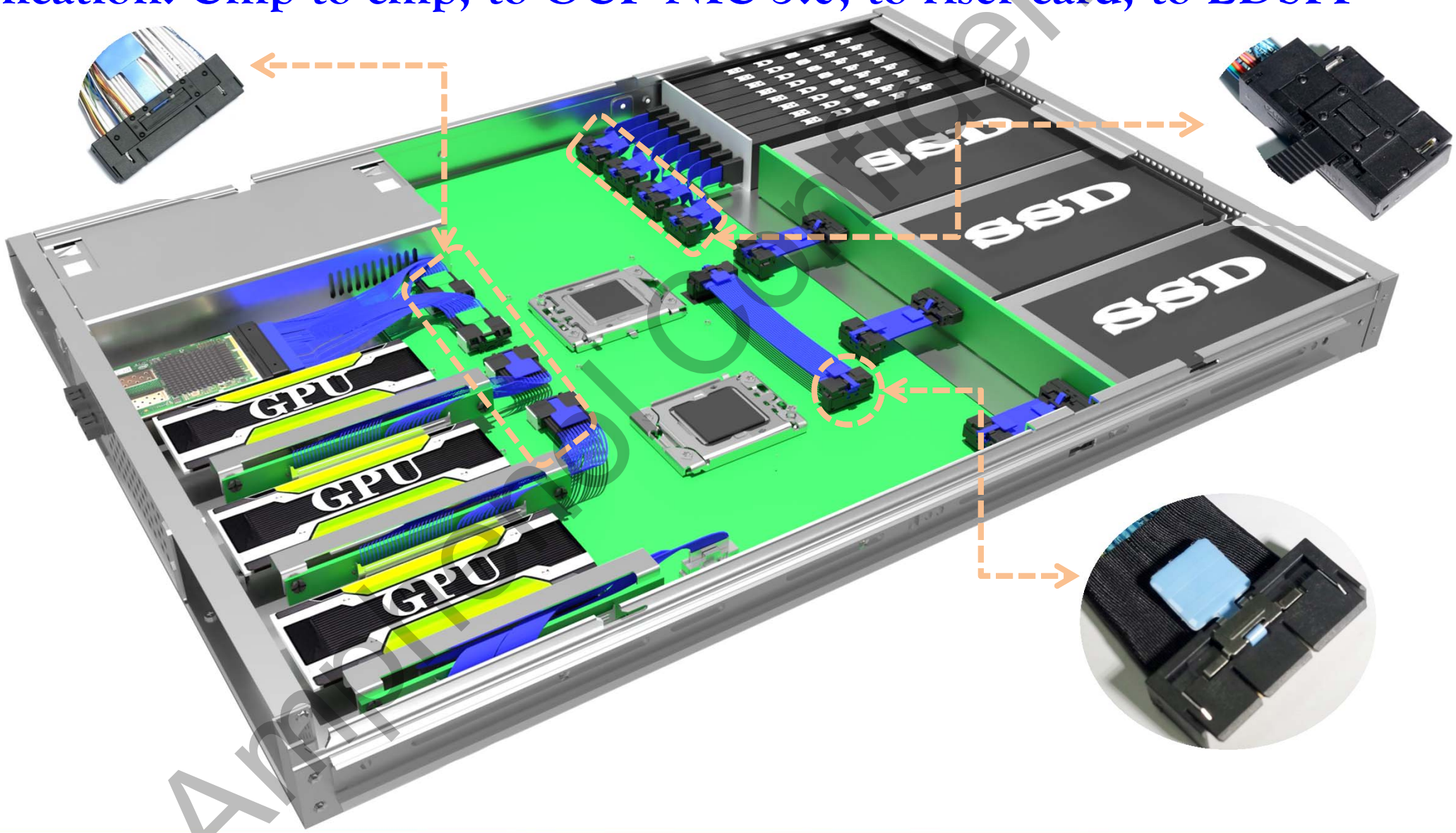
Z-Link(SFF-TA-1020)

Applications: Chip to IO, chip to backplane



Z-Link(SFF-TA-1020)

Application: Chip to chip, to OCP NIC 3.0, to riser card, to EDSFF



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Z-Link(SFF-TA-1020)

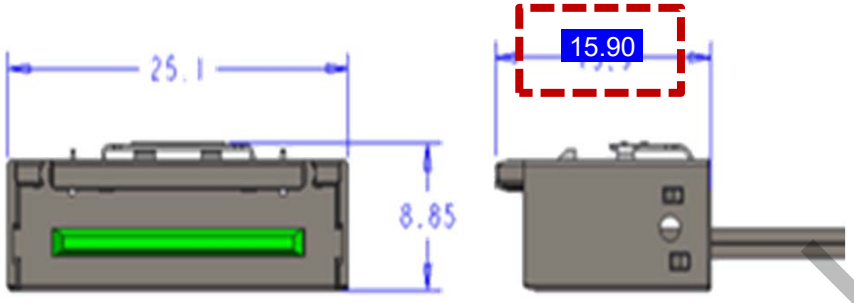
Benefits of application

Industrial Standard	Compliant with SFF-TA-1020, supports OCP and Gen Z
Pin Definition	High speed + power(1.1A/pin) + sideband
Connector Type	Supports 28p(0.5C), 56p(1C), 84p(2C), 140p(4C), 168p(4C+)

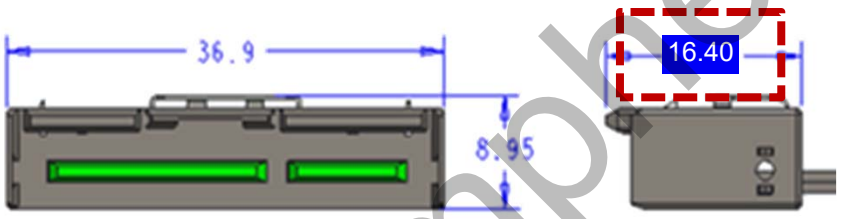
Z-Link(SFF-TA-1020)

Mechanical: Low mating height

Z-Link(SFF-TA-1020)



1C(56pin) STR

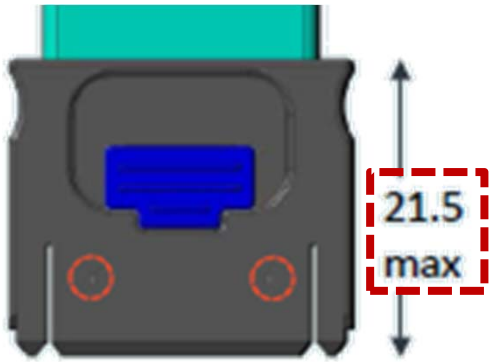


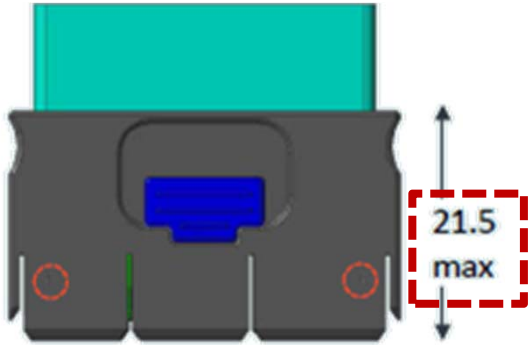
2C(84pin) STR

26% Lower

24% Lower

Standard Gen-Z





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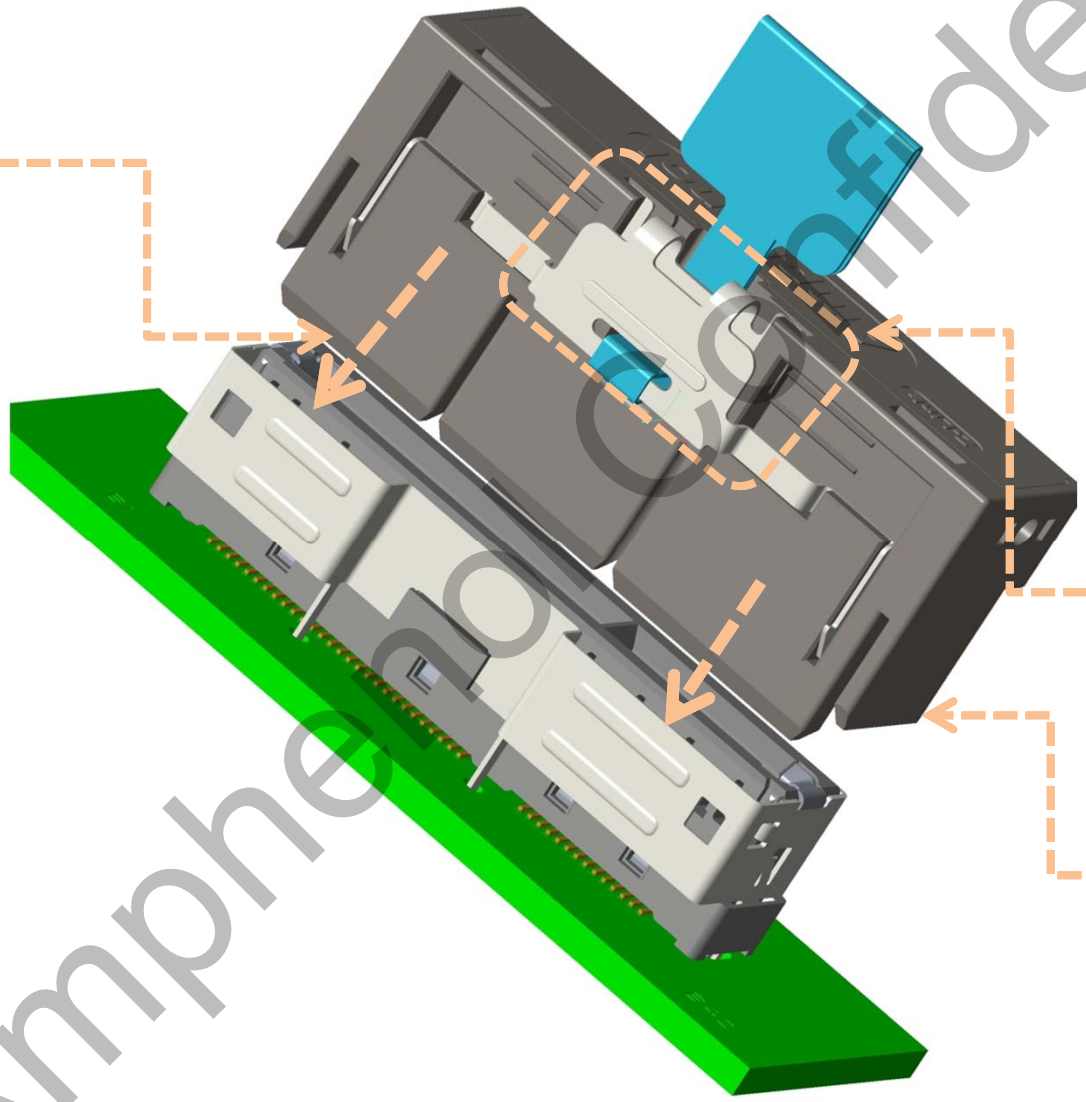
Z-Link(SFF-TA-1020)

Mechanical: Guide in, low profile latch and anti-skew



Amphenol

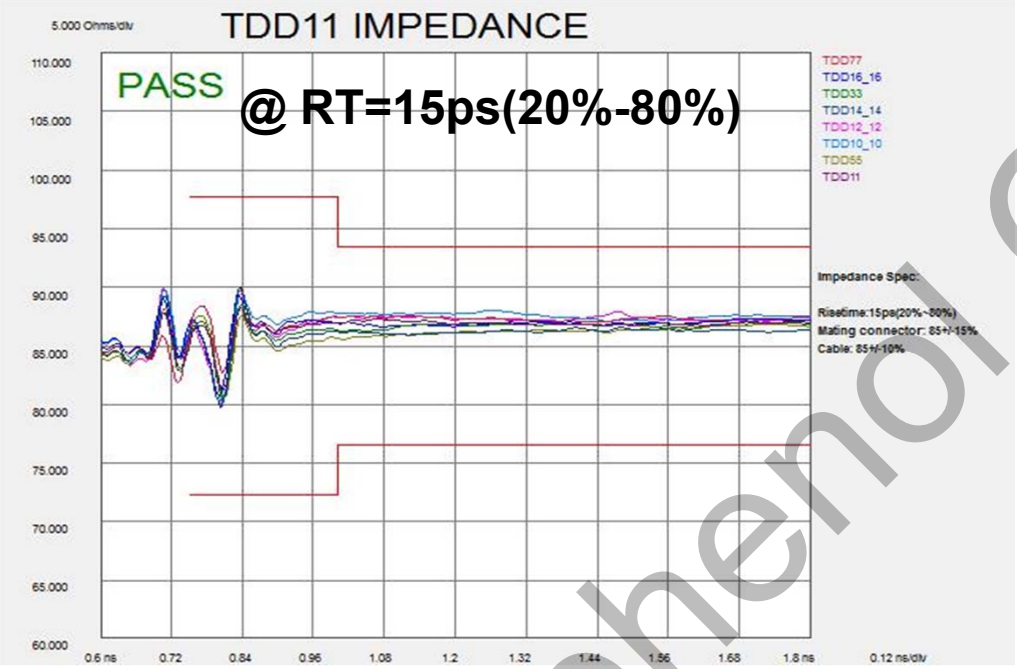
Z-Link(SFF-TA-1020)

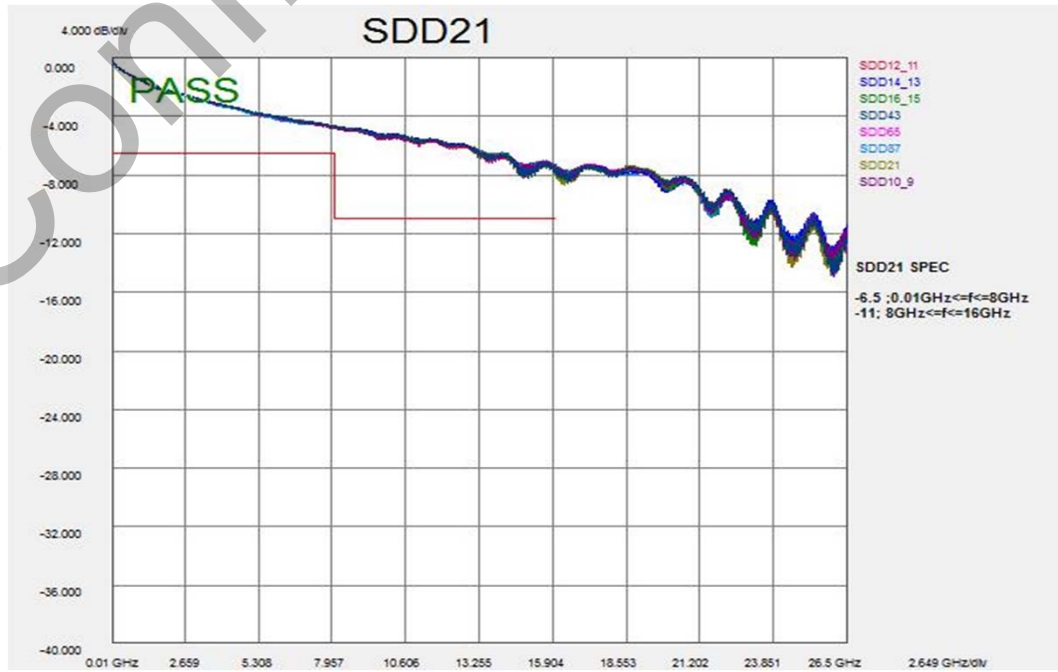
Benefits of mechanical

Robust	Anti-skew features, low profile latch
Small form factor	0.6mm pitch, low profile mating height 16.7mm
Connector type	Plug have RA, STR and SE for different applications

Z-Link(SFF-TA-1020)

SI measured data based on proposed PCIe Gen5 standard, 30AWG 1000mm, STR to STR

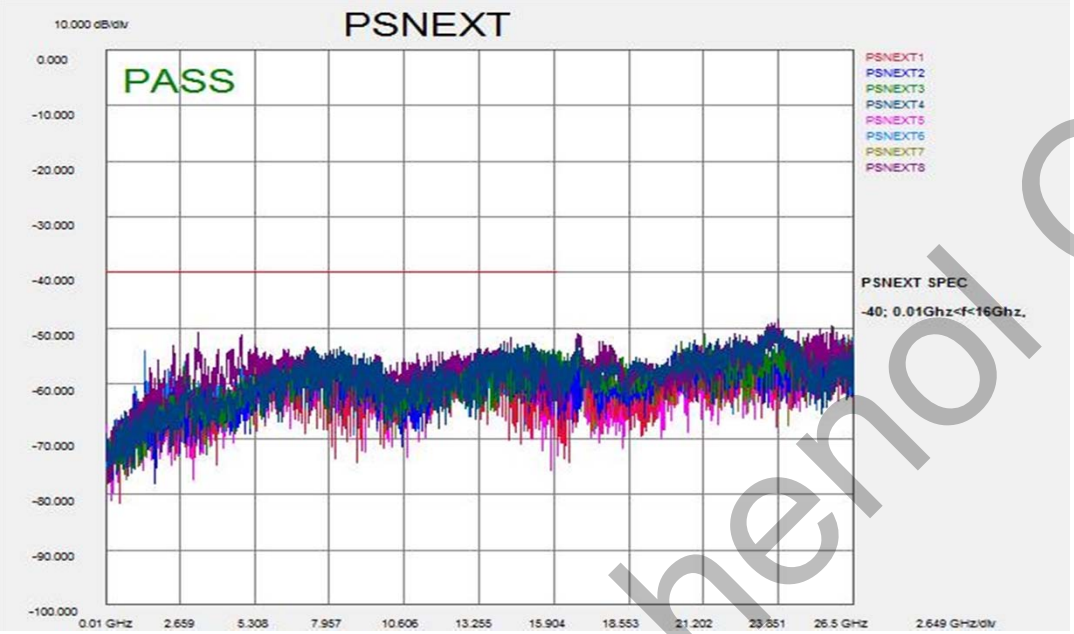


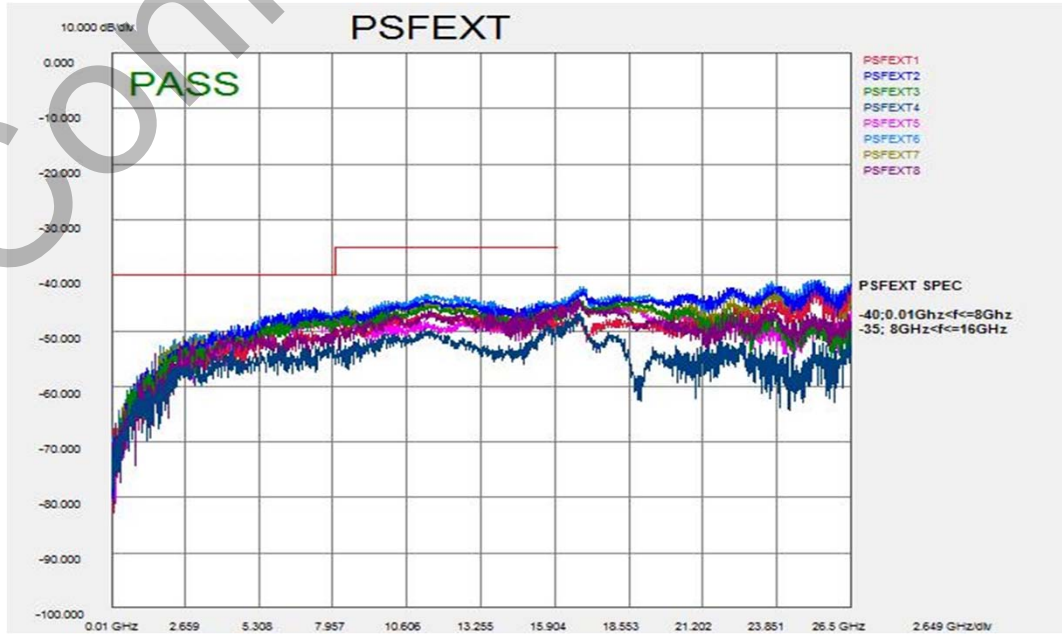


Amphenol

Z-Link(SFF-TA-1020)

SI measured data based on proposed PCIe Gen5 standard, 30AWG 1000mm, STR to STR





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Z-Link(SFF-TA-1020)

Benefits of SI

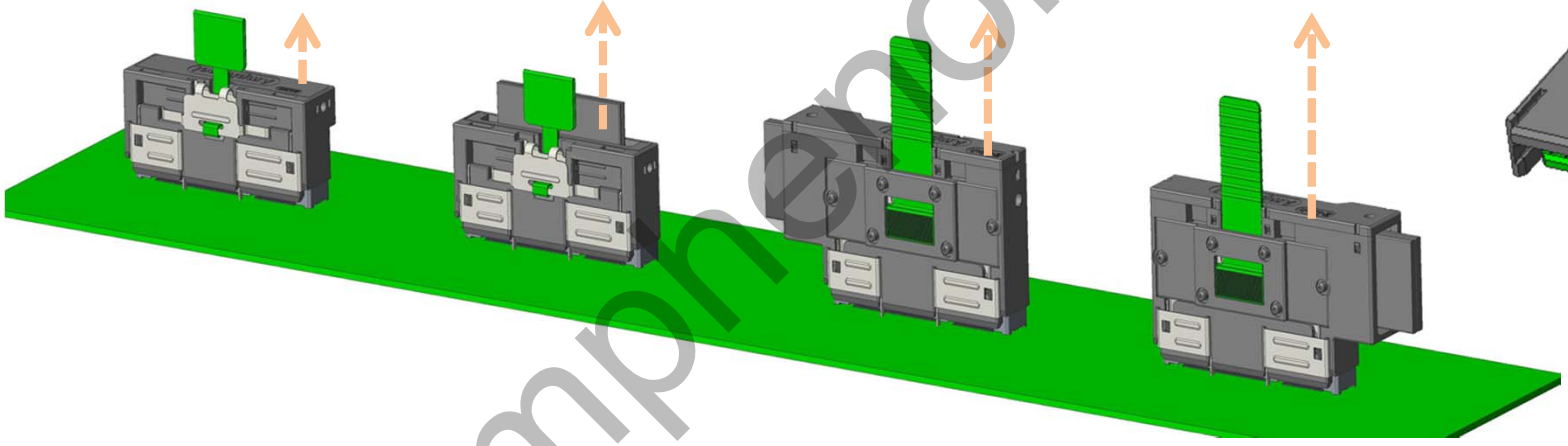
IL	Typical IL is -8.2dB @ 16GHz (1000mm)
Crosstalk	Typical NEXT is -50dB, FEXT is -45dB @ 16GHz
Impedance	Supports 85ohm±10%(RT=15ps)

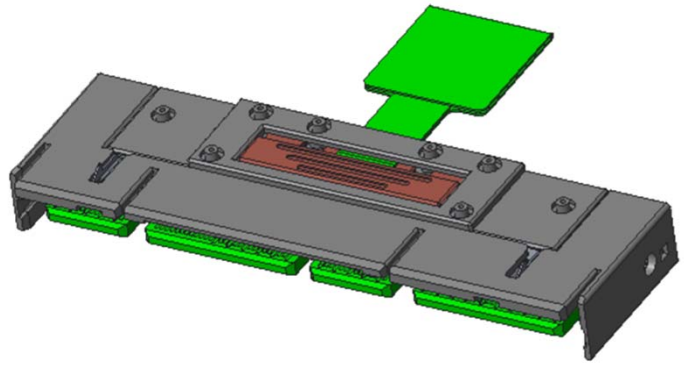
Z-Link(SFF-TA-1020)

Configuration matrix

Types	0.5C	1C	2C	4C	4C+
Pin no.	28pin	56pin	84pin	140pin	168pin
Channels	4X	4X+SB+P	8X+SB+P	16X+SB+P	16X+SB+P
Status	STR Available	Available			STR/RA/RSE Available

Z-Link RA Z-Link STR Z-Link LSE Z-Link RSE





Z-Link 4C+

Note: Pull tab color could be optional: Blue and Green

Z-Link(SFF-TA-1020)

Highlight

Protocol
- Supports proposed PCIe Gen5 standard, SFF-TA-1020 and OCP

Mechanical
- Robuster, anti-skew feature, low profile latch

Application
- Chip to riser, chip to IO, chip to backplane, chip to chip

Ultraport SlimSAS LP

SlimSAS LP

SlimSAS LP is a low-profile form factor solution of SlimSAS with a mating height is 11.3mm(for special application), with footprints compatible with SlimSAS, adopted by UPI 1.0 and support PCIe Gen5.

SI

- **Supports proposed PCIe Gen5, SAS4.0 and UPI1.0**

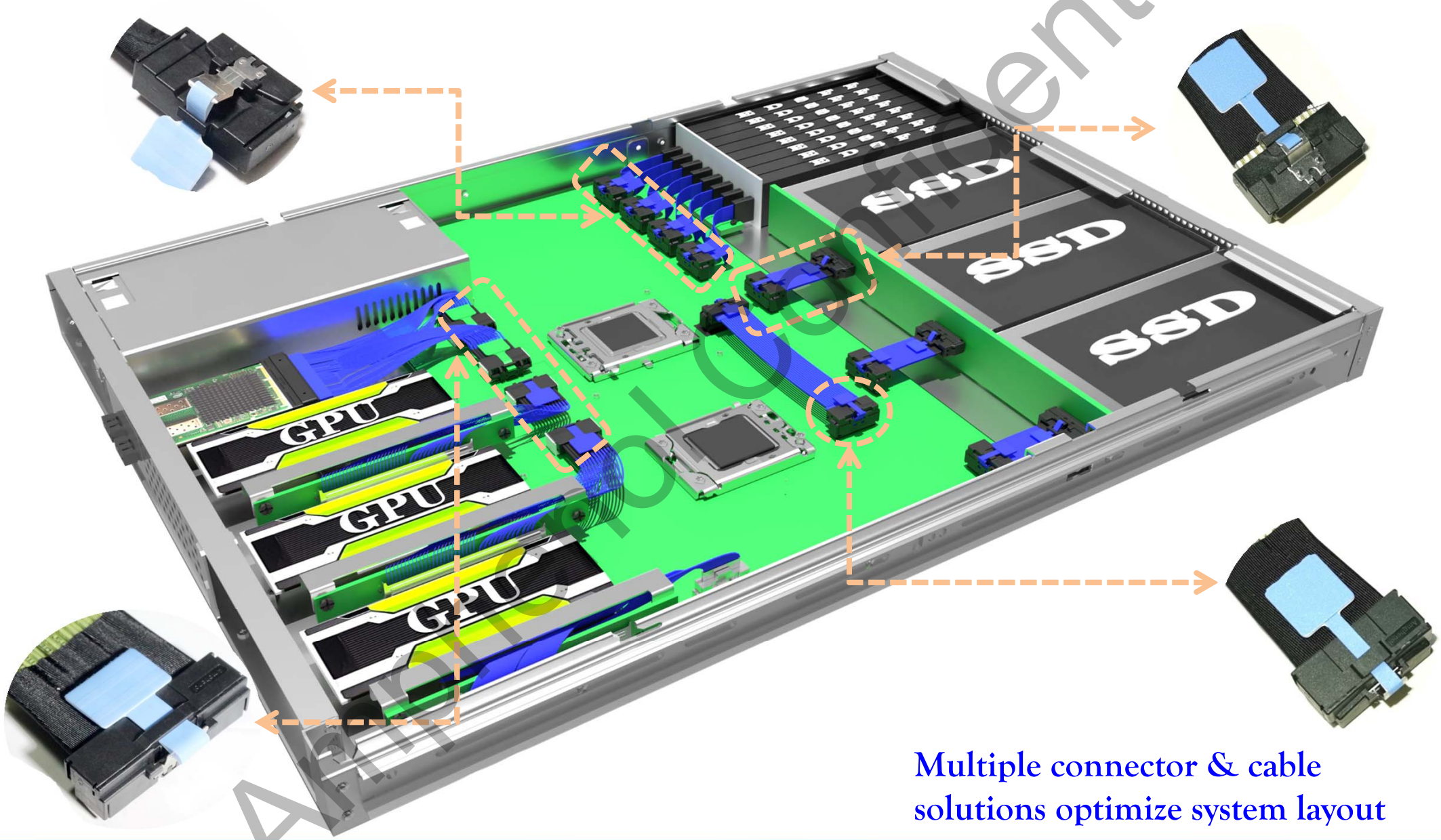
Mechanical

- **Footprint compatible with SlimSAS, anti-skew feature**

Application

- **Supports Chip to riser card, chip to chip, chip to backplane**

SlimSAS LP



Multiple connector & cable solutions optimize system layout

Amphenol

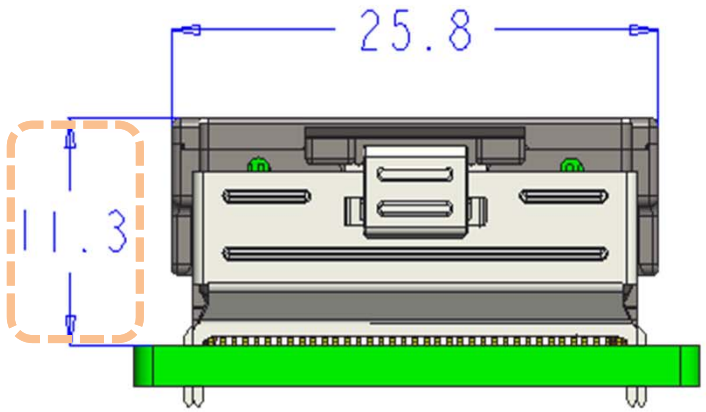
SlimSAS LP

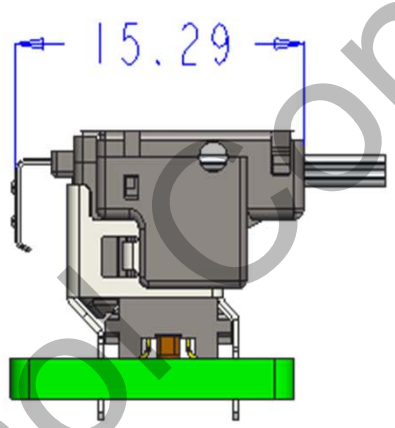
Benefits of application

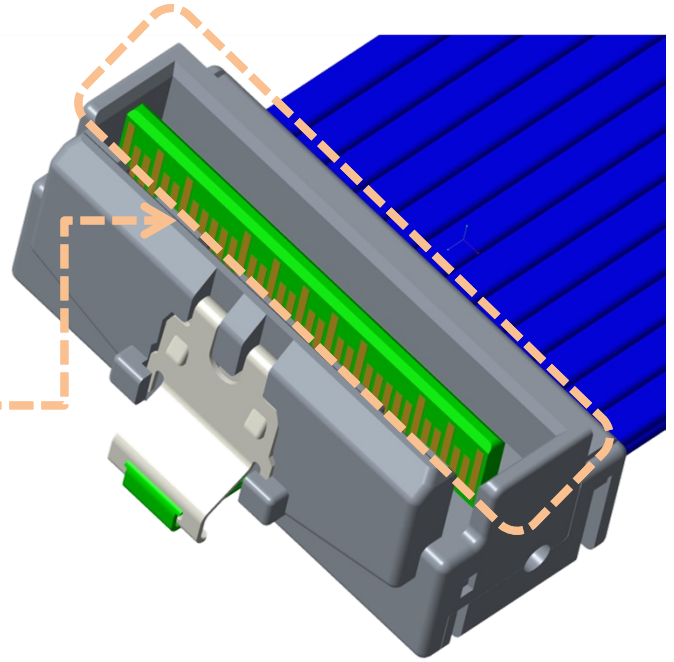
SI	Supports proposed PCIe Gen5 standard, SAS4.0 and UPI1.0
Layout	Footprint compatible with standard SlimSAS
Connector type	Pull tab and long latch is optional for narrow layout

SlimSAS LP

Mechanical: Mating height 11.3mm is customized for special application and 74pin sample is available.







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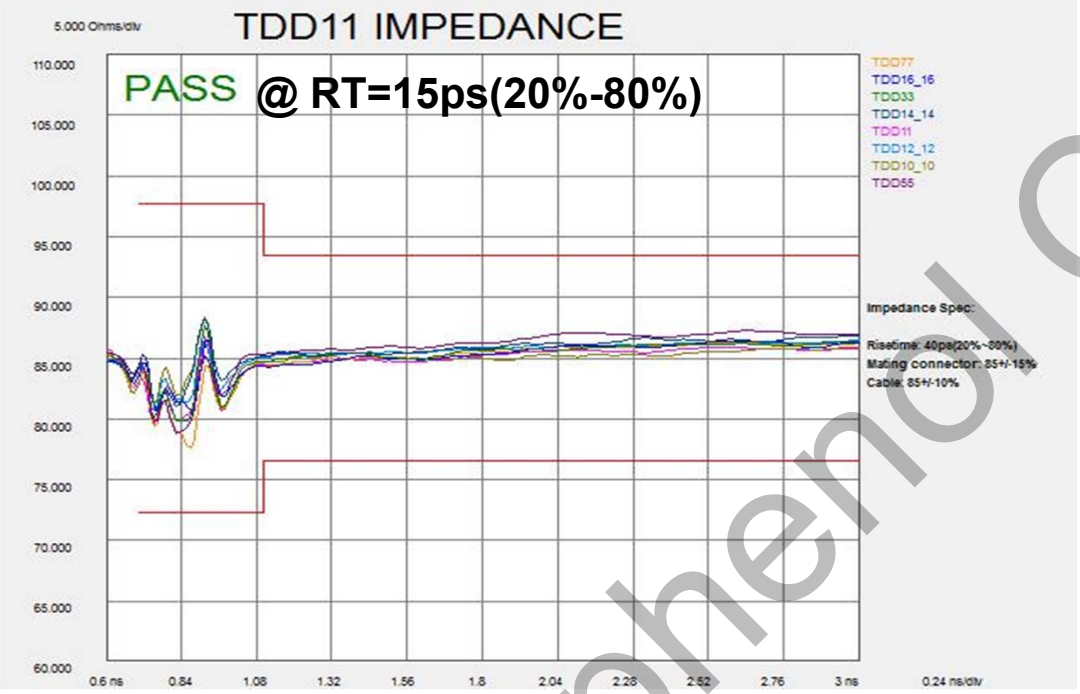
SlimSAS LP

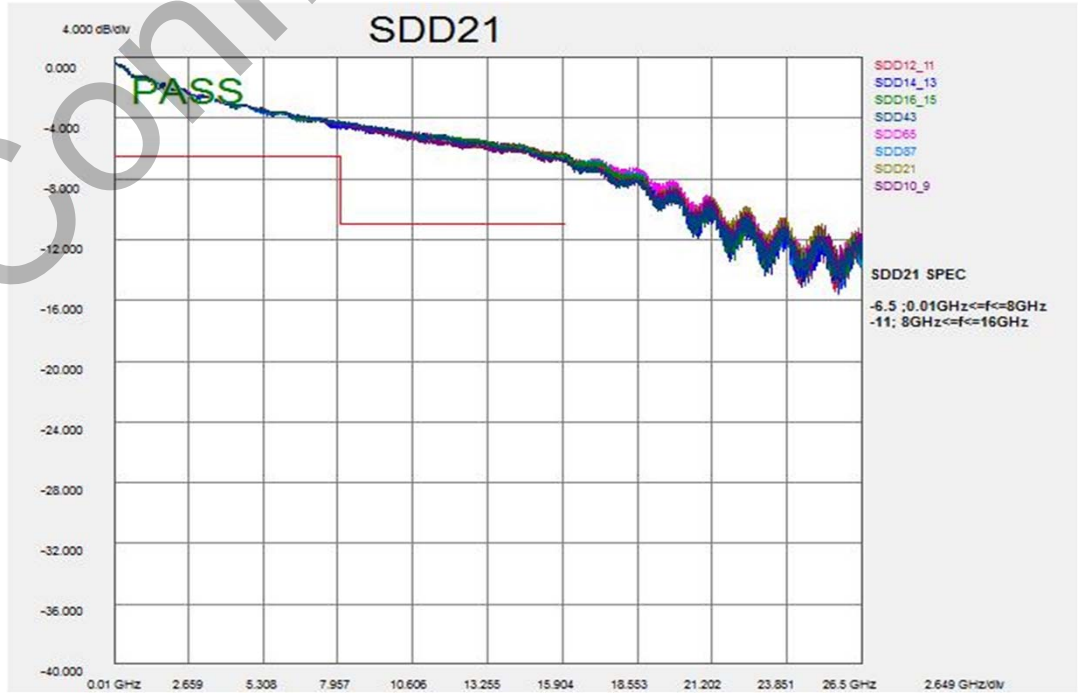
Benefits of Mechanical

Robust	Anti-skew feature
Small size	0.6mm pitch, low profile mating height 11.3mm for special application
Connector type	38p, 74p and 124p with RA, STR and SE

SlimSAS LP

SI measured data based on proposed PCIe5 standard, 30AWG 1000mm, V/T with STR plug





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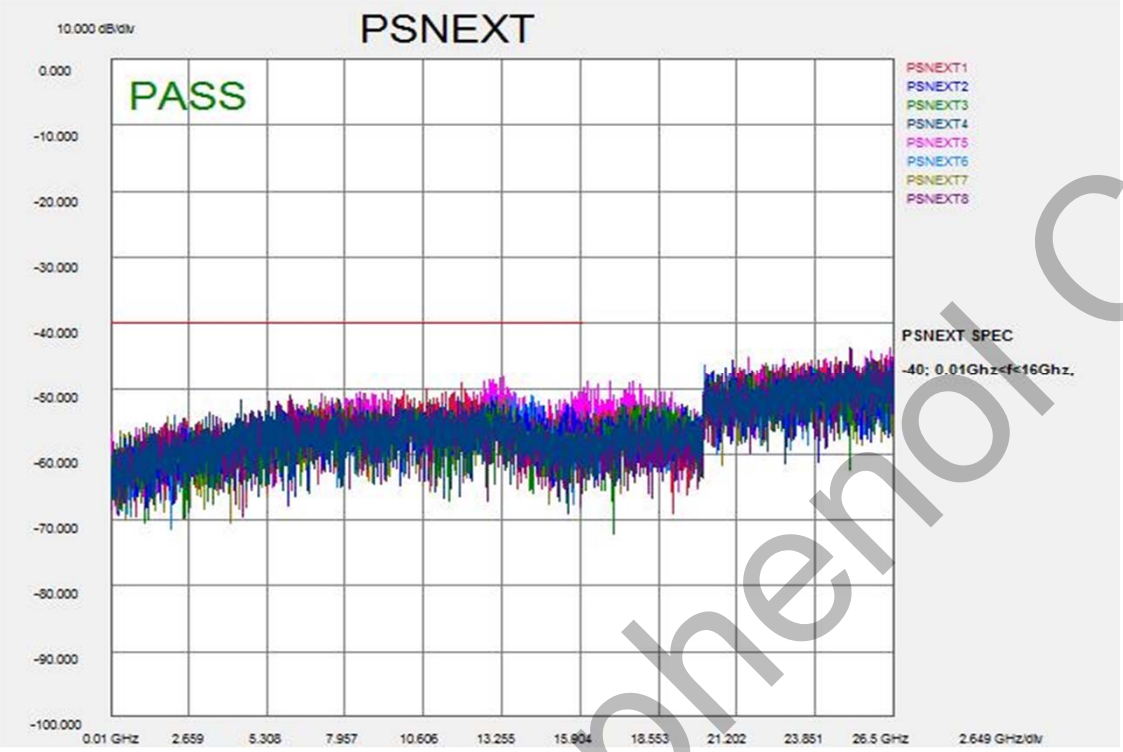
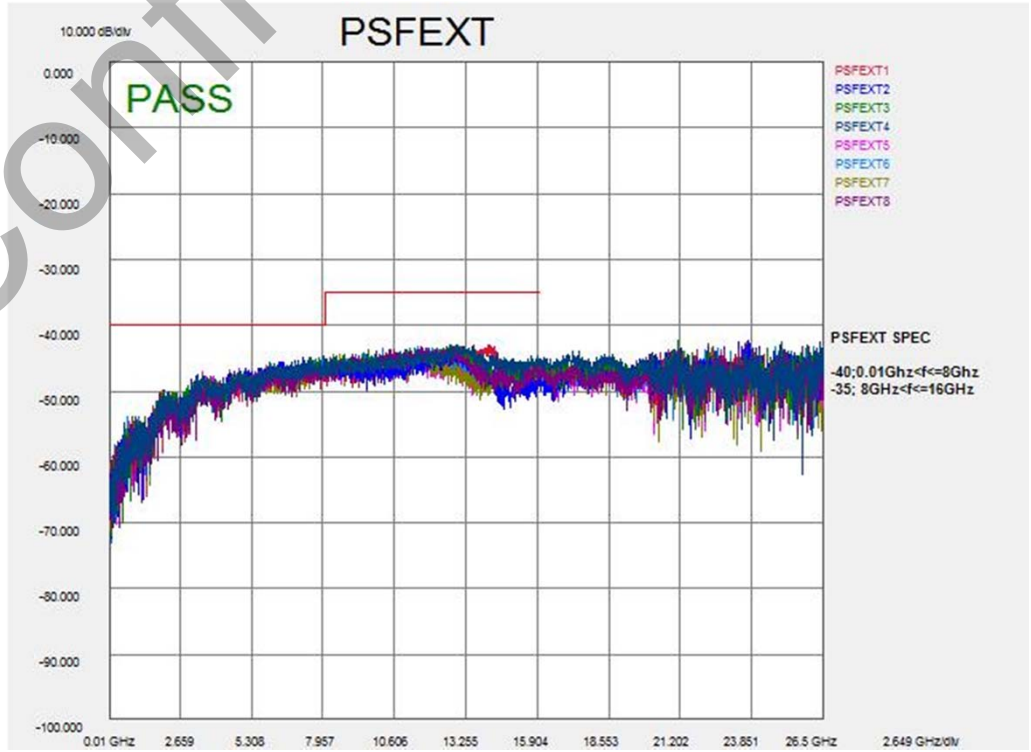
SlimSAS LP

SI measured data based on proposed PCIe5 standard, 30AWG 1000mm, V/T with STR plug





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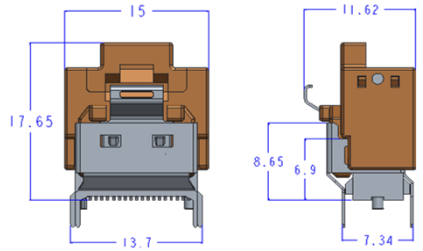
SlimSAS LP

Benefits of SI

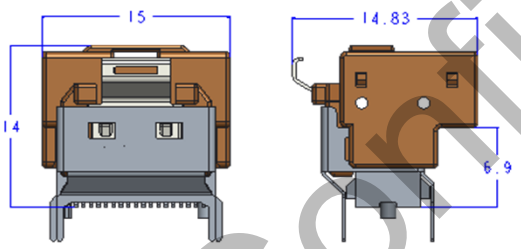
- **IL** — Typical IL is -7dB @ 16GHz (1000mm)
- **Crosstalk** — Typical NEXT is -48dB, FEXT is -45dB @ 16GHz
- **Impedance** — Supports 85ohm±10% (RT=15ps)

Configuration matrix

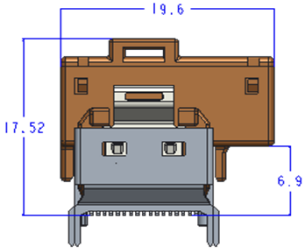
4X(38pin) Straight



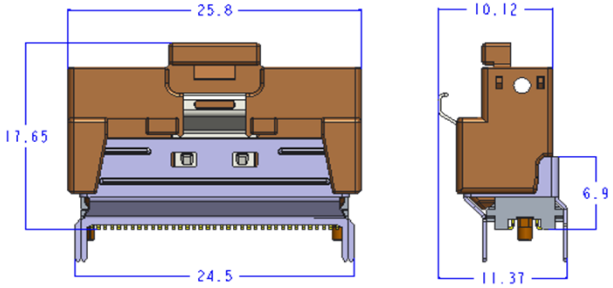
4X (38pin) Right Angle



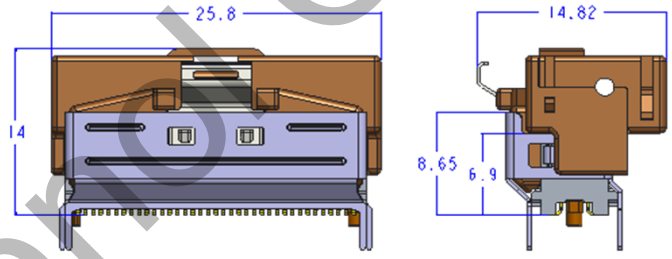
4X(38pin) Side-exit



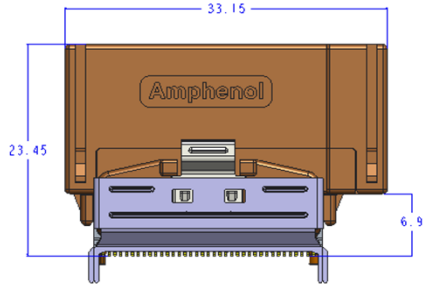
8X(74pin) Straight



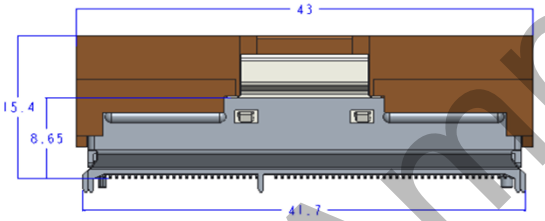
8X(74pin) Right Angle



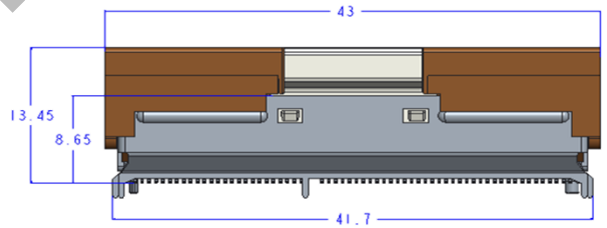
8X(74pin) Side-exit



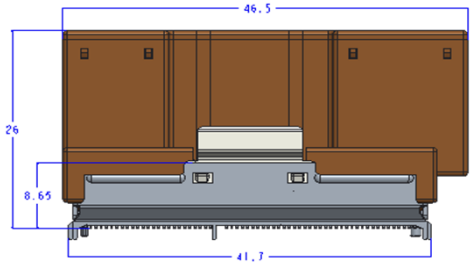
16X+SB (20X,124pin) Straight



16X+SB (20X,124pin) Right Angle



16X+SB (20X,124pin) Side-exit



SlimSAS LP

Highlight

Protocol
- Supports proposed PCIe Gen5 standard, SAS4.0, UPI1.0

Mechanical
- Robuster, anti-skew, footprint compatible with SlimSAS

Application
- Supports chip to backplane, chip to riser, chip to chip

Extremeport-Flash

Flash

Flash is one of lowest mating height solution for chip to IO application. Mating height is 4.50mm, date rates up to 56G PAM4 and available with both side latch and lock bar latch.

SI

- Supports SFF-TA-1002 56G PAM4 spec
- Scalable to support SFF-TA-1002 112G PAM4 spec

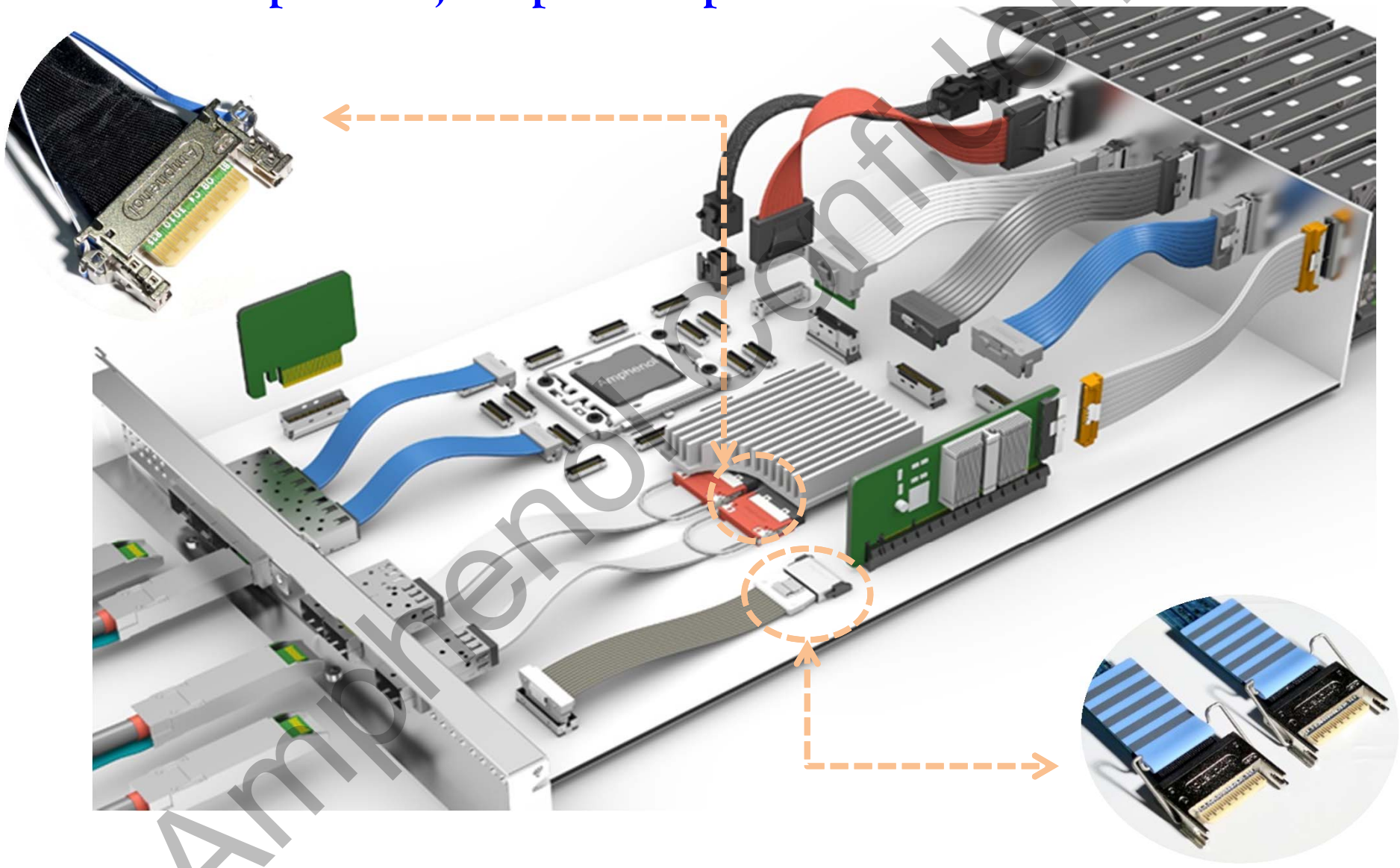
Mechanical

- Lock bar latch and side latch are available

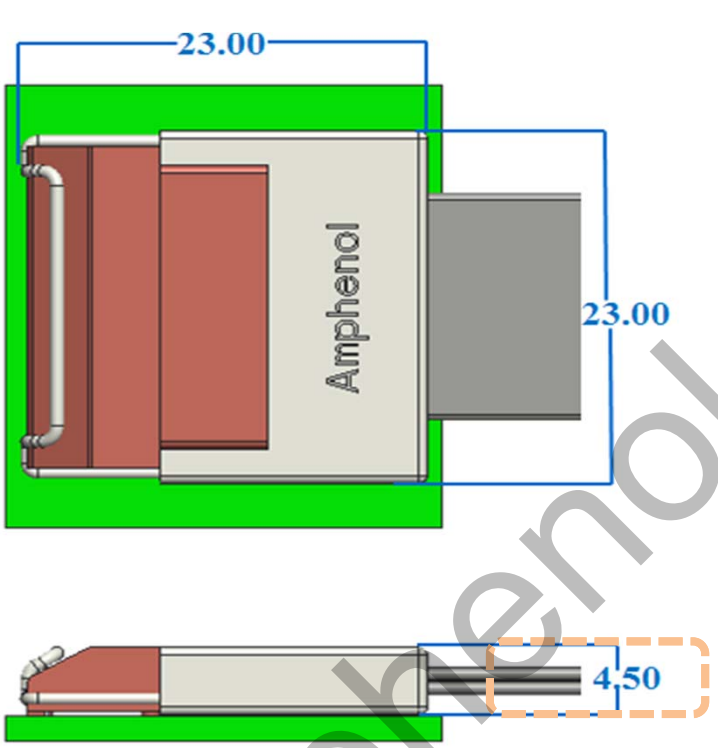
Application

- Supports chip to IO, chip to chip with 95ohm

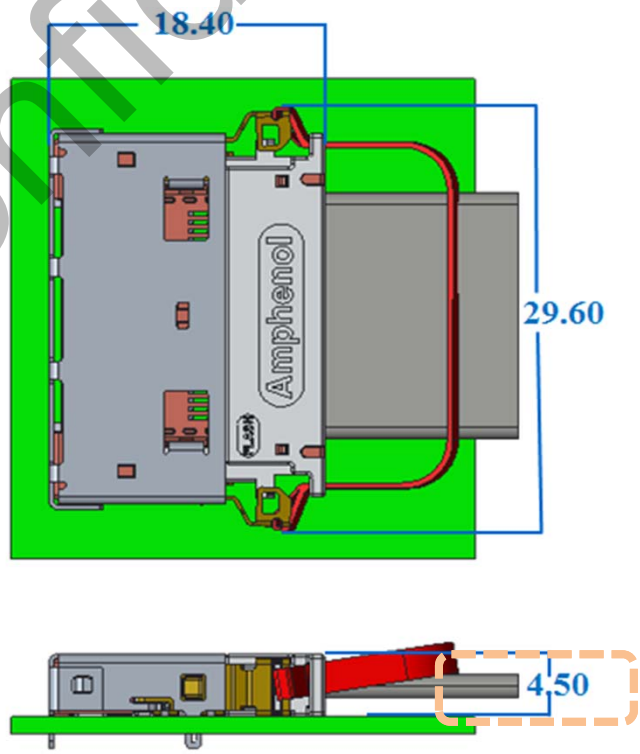
Applications: chip to IO, chip to chip



Mechanical: Low mating height

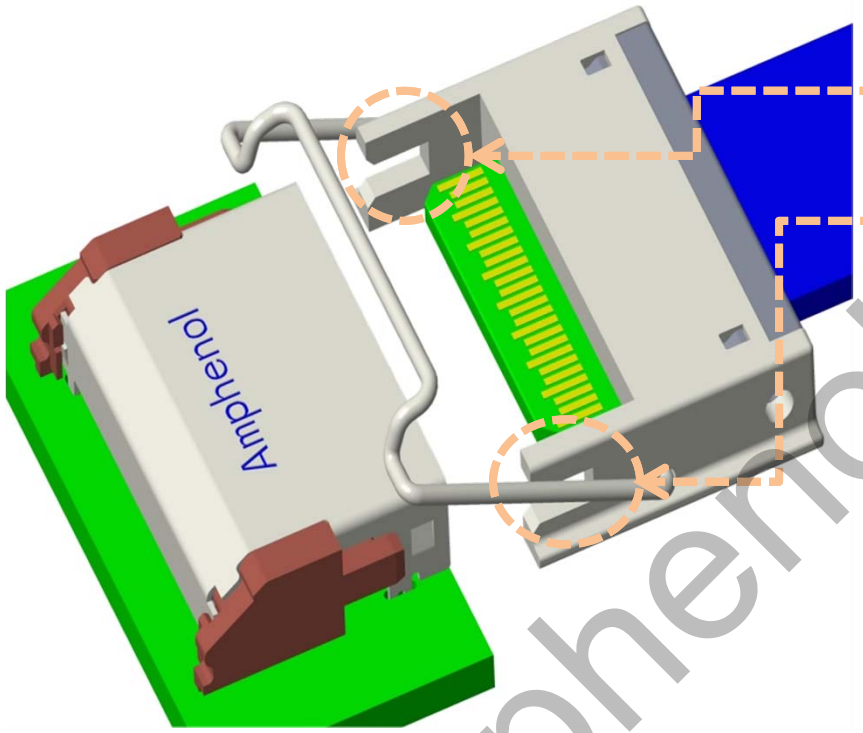


Flash1.0 8X(50pin)

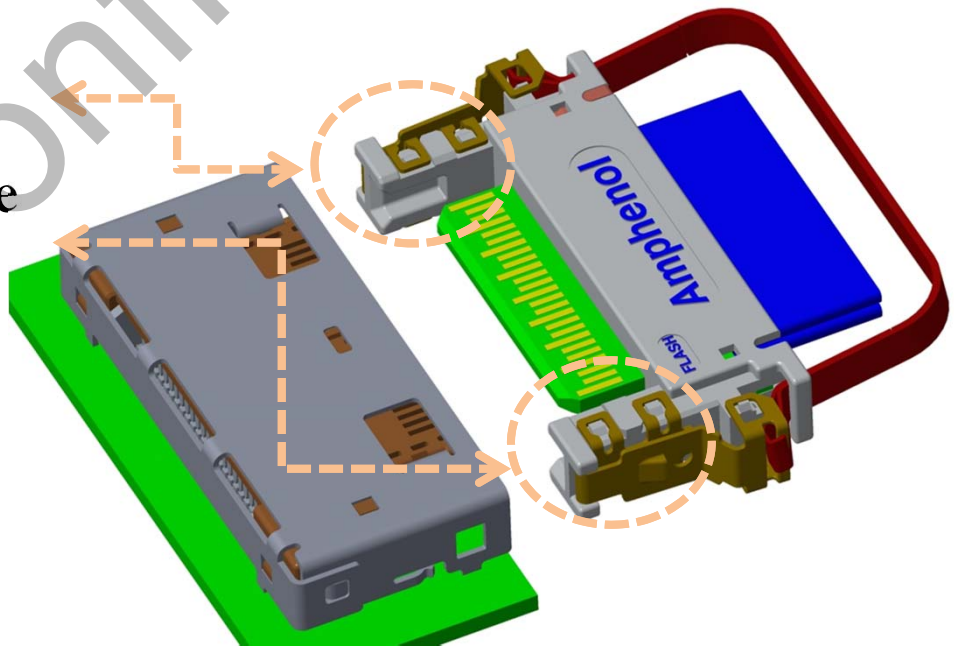


Flash2.0 8X(50pin)

Mechanical: Guide feature



Guide feature



Flash1.0 8X(50pin)

Flash2.0 8X(50pin)

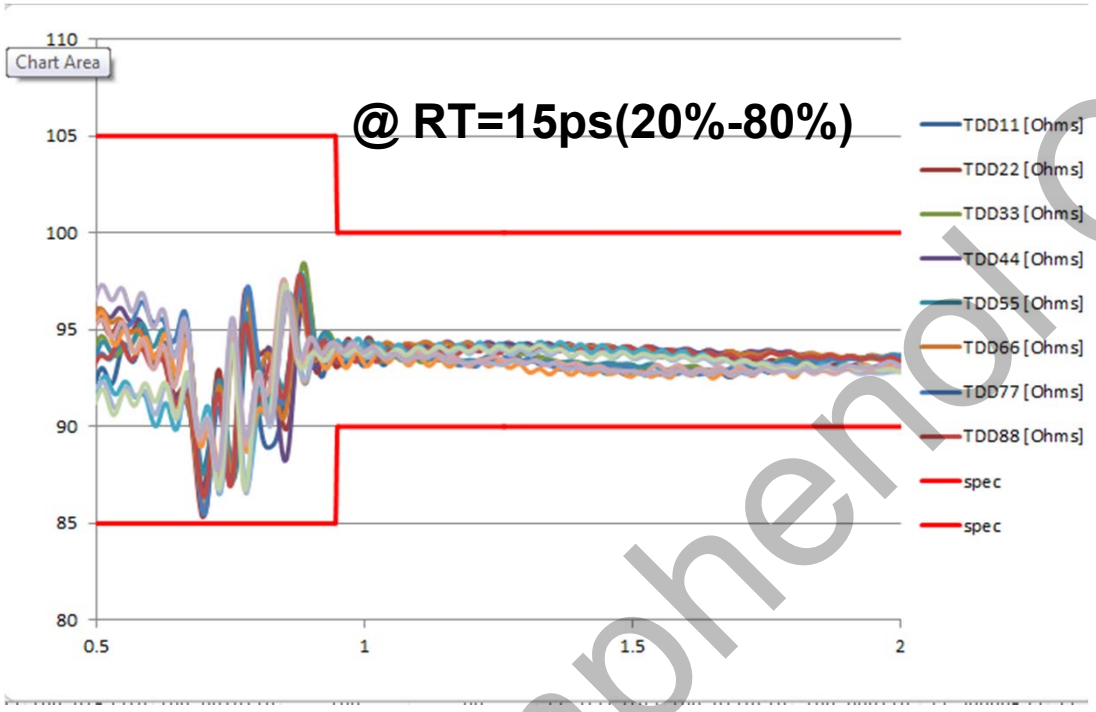
Flash

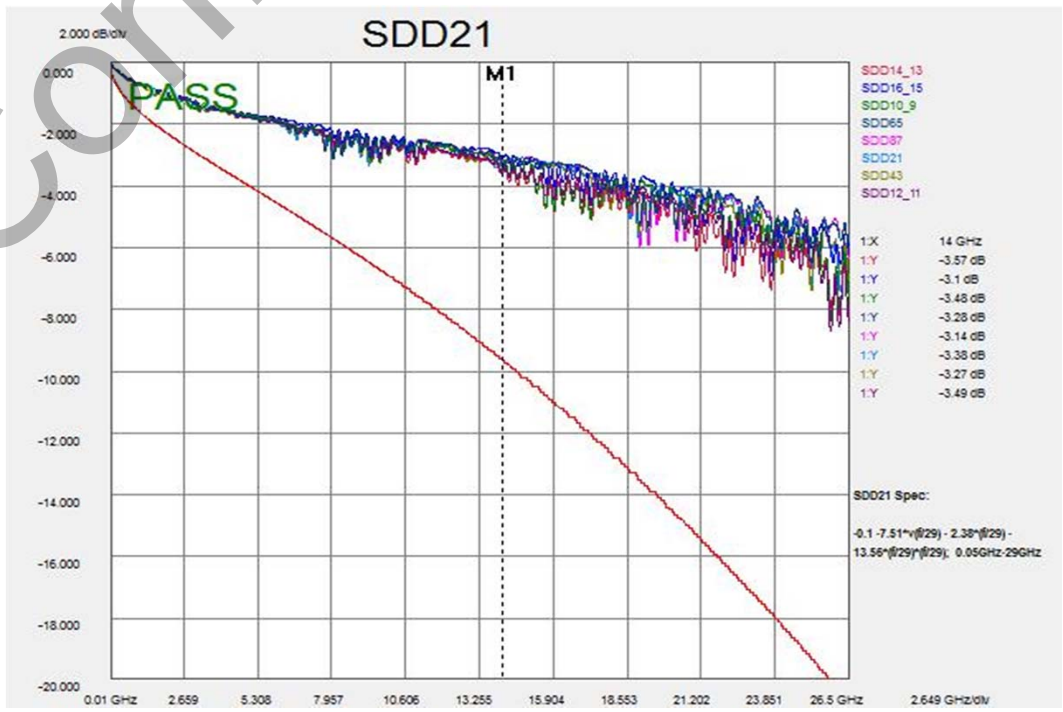
Benefits of mechanical

Mechanical	Robuster, Guide feature
Mating height	0.6mm pitch, extreme low mating height 4.5mm
Connector type	Lock bar and side latch are optional for different applications

Flash

SI measured data based on TA1002 56G PAM4 spec, 30AWG 300mm, R/A receptacle with STR plug

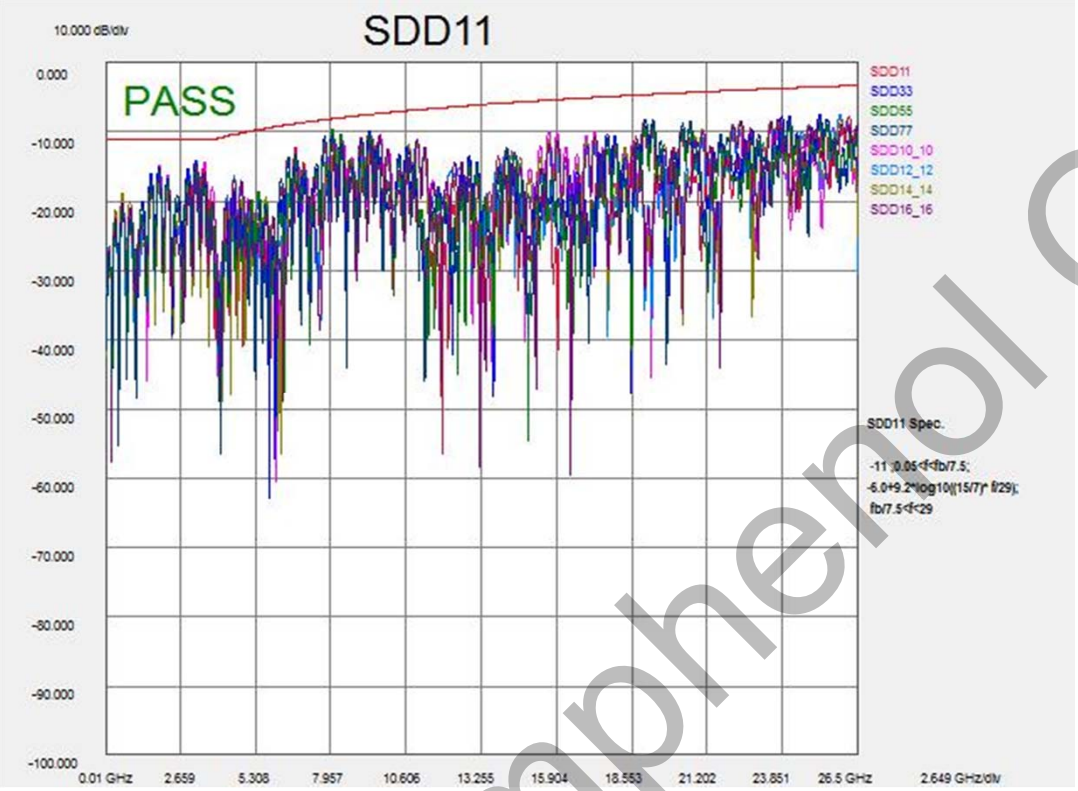


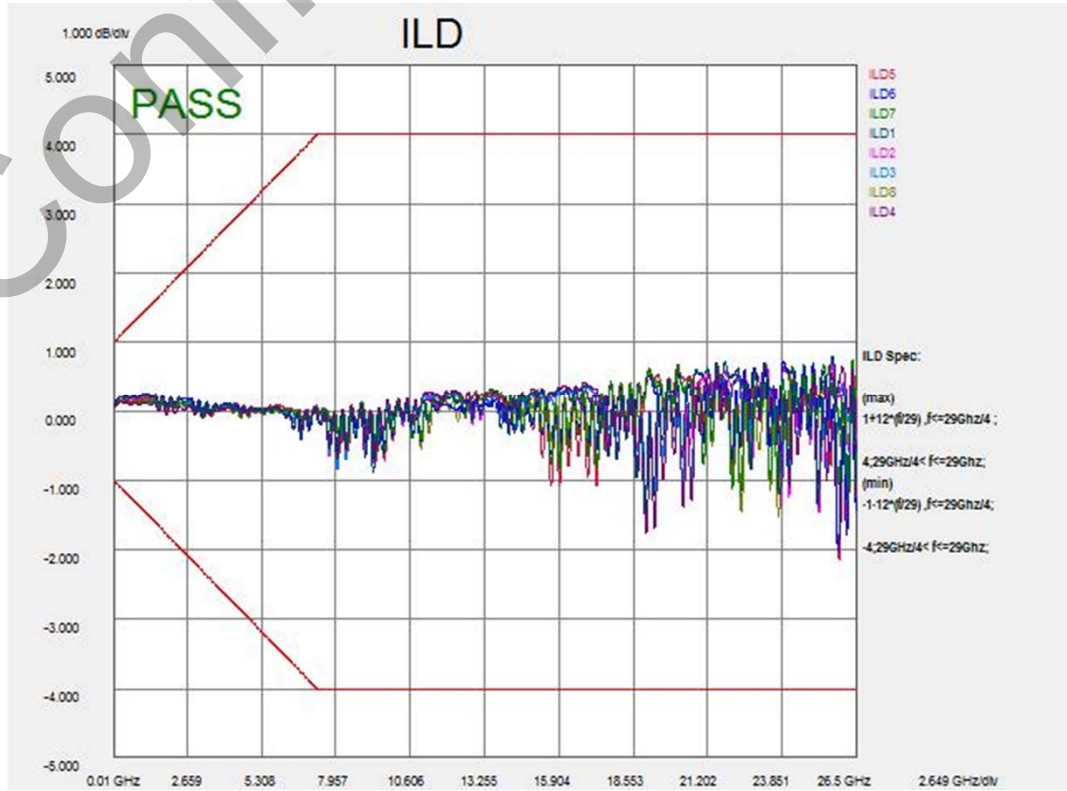


Amphenol

Flash

SI measured data based on TA 1002 56G PAM4 spec, 30AWG 300mm, R/A receptacle with STR plug

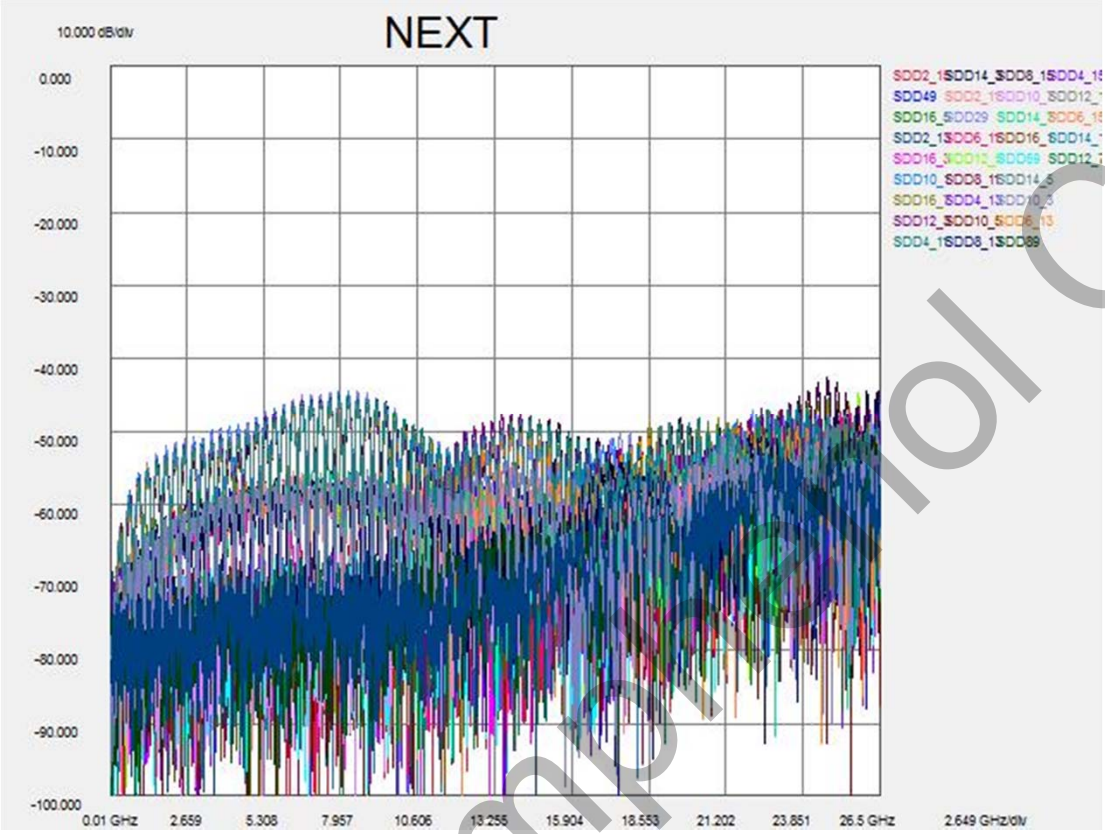


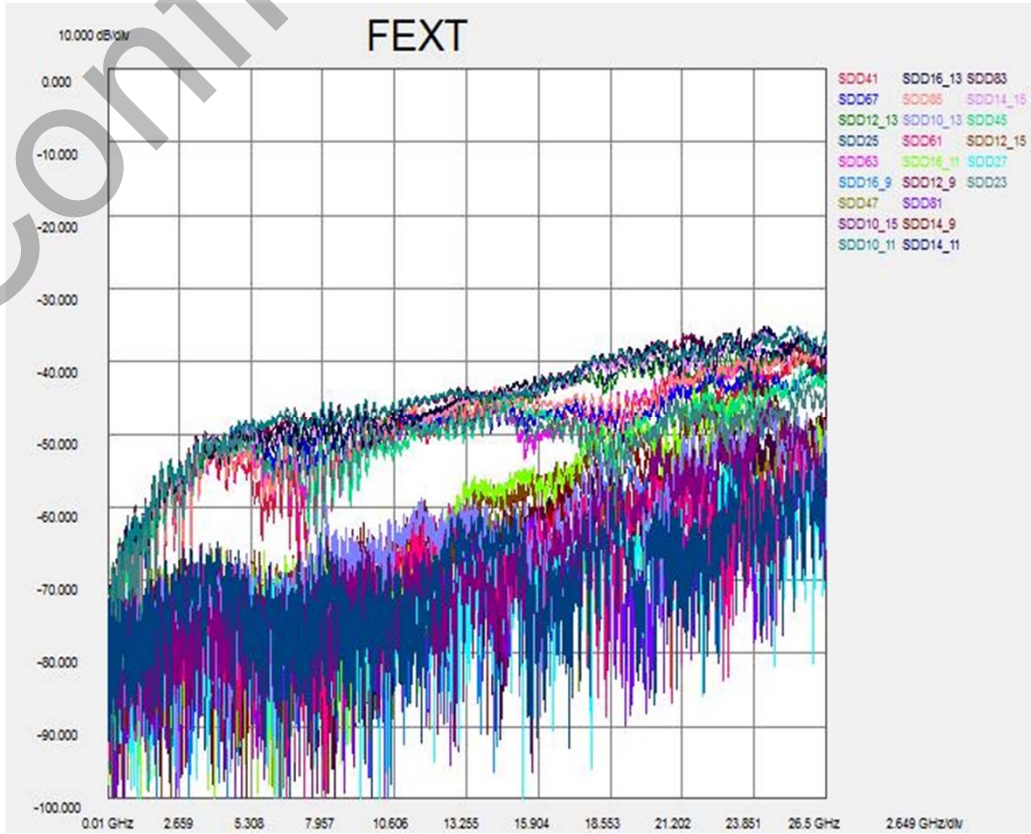


Amphenol

Flash

SI measured data based on TA1002 56G PAM4 spec, 30AWG 300mm, R/A receptacle with STR plug





Amphenol

Flash

Highlight

Protocol

- Supports SFF-TA-1002 56G PAM4 spec
- Scalable to SFF-TA-1002 112G PAM4 spec

Mechanical

- Guide feature, side latch and lock bar latch

Application

- Chip to IO, chip to chip with 95ohm

Thank You

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